Regulator Isolation and PowerStic-Exodus Operation

Voltage regulator manufacturers specify their devices in terms of forward transfer (S21) or, unregulated input to regulated output performance characteristics. Little to nothing is defined in terms of reverse regulator isolation, or S-parameter S12. Further, there is very little regulator performance information at frequencies above and beyond 10 MHz, in the forward or reverse direction.

Is it of any importance how well voltage regulators isolate activity occurring at their outputs from their inputs? Generally, this subject has been considered "leakage" in the system, and has not been studied. With the advent and production of the CurrentRF PowerStic and Exodus devices, it has been discovered that capturing and harnessing this leakage can be a source of considerable harvested power.

This paper presents measured data gathered on linear and switch mode regulators with respect to broadband reverse regulator isolation. Regulator manufacturer data sheet information is examined in light of device measured reverse isolation, and collected data is correlated to the published data found in regulator manufacturer datasheets.

Linear Regulators

Although there is a plethora of linear voltage regulator designs in today's marketplace on a variety of processes, one can roughly categorize them into two very broad categories, series pass and low drop out (LDO).

Linear Series Pass Linear Regulators

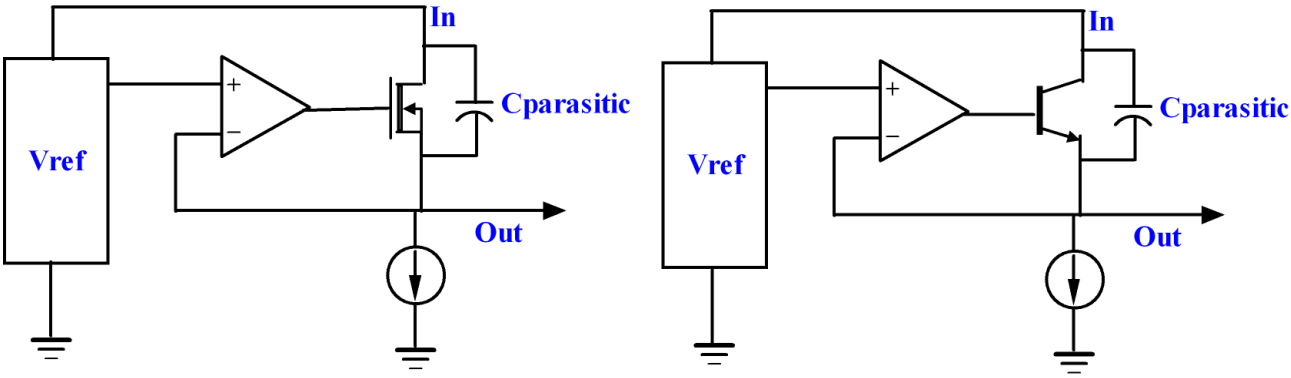


Figure 1: Linear Series Pass Regulator Architecture

Figure 1 shows the basic architecture of a linear series pass regulator. Generally, the regulator consists of a fixed reference (Vref) and a Fet or a bipolar transistor controlled and driven by a negative feedback loop containing a high gain element (Op Amp). Usually, a current source is utilized to bias the series pass element in the architecture, but can be omitted in low power applications. The Cparasitic element in the above architecture is generally ignored in most applications, but is important when considering the effects of high frequency reverse isolation in regulators.

Basic Models

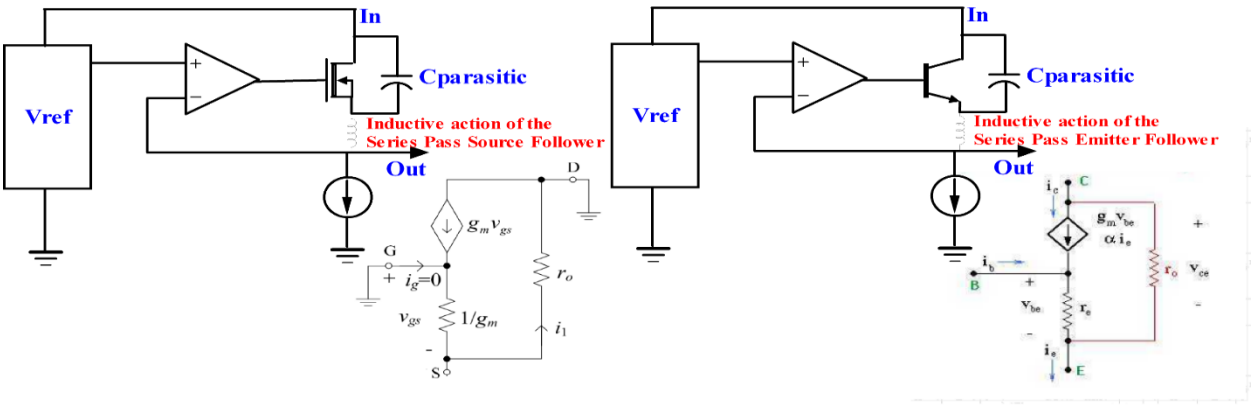


Figure 2: Linear Series Pass Regulator Models

The series pass element in the architectures shown in Figures 1 and 2 determine the high frequency reverse isolation characteristics of the series pass regulator. Small signal hybrid T modeling is appropriate for use here, in that the small signal dynamic characteristics of the series pass transistor set the reverse isolation performance of the regulator in this configuration. The series pass architecture has an inductive characteristic (see figures 2 and 3) due to the embedded emitter/source follower transistor configuration. At DC or frequencies at or below the unity gain bandwidth of the control Op Amp, the control loop forces the gate/base of the series pass transistor to track the events at the source/emitter, thus cancelling the follower inductive effect. At frequencies above the unity gain bandwidth of the control Op Amp, however, the series pass element in the architecture is free to react to current changes through the series pass transistor, acting much like an embedded inductor in series with the transistor source/emitter and the output node of the regulator.

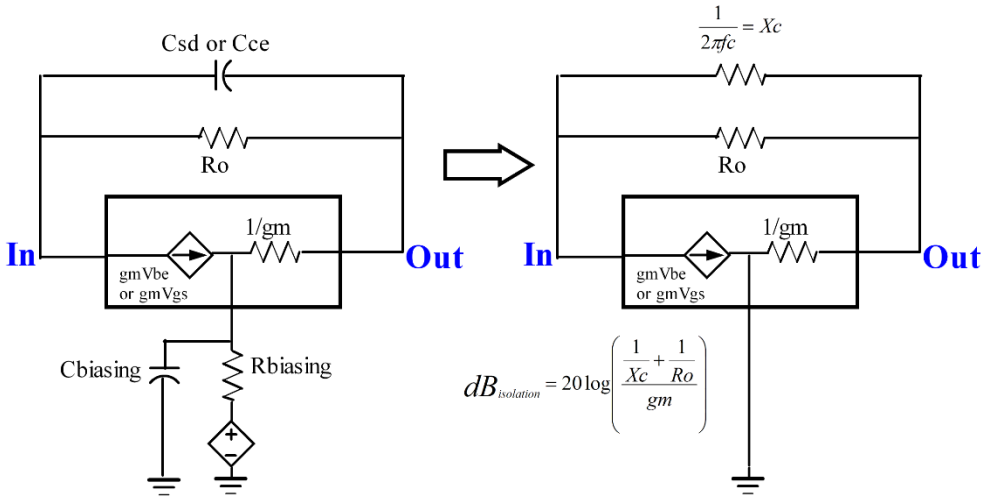
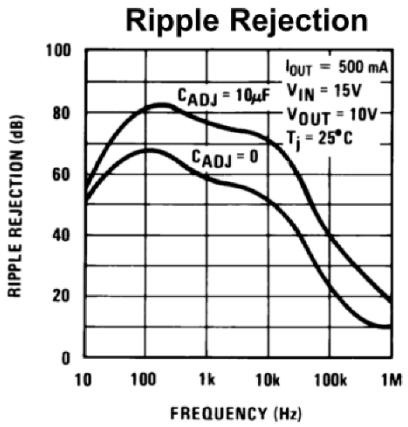


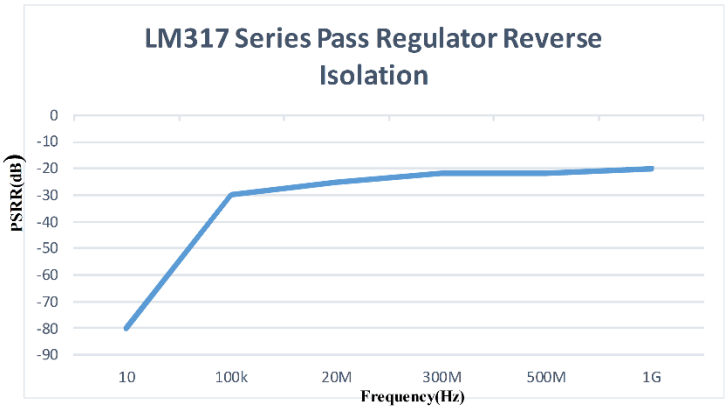
Figure 3: Linear Series Pass Regulator Macro Model

The simplified models of Figure 3 show the elements involved and the mathematical relationship as it relates to regulator reverse isolation. The model shown in Figure 3 shows a simple high frequency relationship between the output resistance of the series pass element (Ro), the frequency response of the bridging capacitance (Xc), and the gm of the series pass element in the architecture. The result is the reverse isolation of the regulator, expressed in dB.

Referring to Figure 3, as Xc or gm of the device increases, the reverse isolation of the regulator increases. Thus at relatively low noise frequencies, Xc, the reactance of the bridging capacitor, increases, lowering the overall conductance, forcing currents through the series pass device, changing the gm, changing the device Vgs /Vbe, causing the device's inductive effect. As frequencies increase, Xc decreases, increasing the bridging conductance, decreasing the device gm change, thus decreasing the series pass device inductive effect. As frequencies increase further, the Xc of the bridging capacitance becomes low enough so as to compete with the 1/gm input resistance of the series pass device, thus further decreasing the inductive effect of the of the series pass device. This "break point" can be adjusted by either increasing the bridging capacitance value, or increasing the DC current through the regulator series pass device, thus increasing its gm.

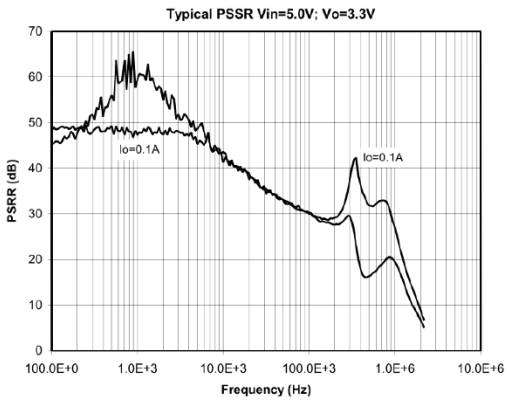


LM317 Series Pass Regulator PSRR

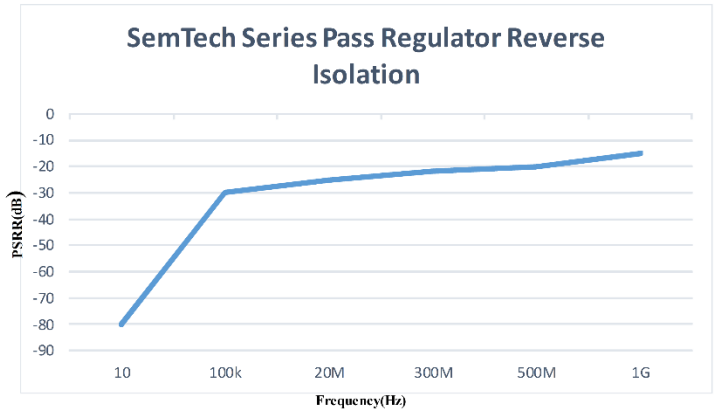


LM317 Series Pass Regulator Measured Reverse Isolation

Figure 4: National LM317 PSRR and Reverse Isolation



Semtech Native Series Pass Regulator PSRR



Semtech Native Series Pass Regulator Measured Reverse Isolation

Figure 5: Semtech SC4215A PSRR and Reverse Isolation

These effects are graphically displayed in in Figures 4 and 5. Two series pass regulators, the National LM317 and Semtech SC4215A (schematics and block diagrams shown in Figures 6 and 7) are shown to have excellent PSRR (reverse isolation) out to about 1 MHz. The PSRR/Reverse Isolation starts to degrade at frequencies greater than 1 MHz, ranging between -30dB at 1 MHz to -10dB at 1 GHz. The bipolar LM317 seems to have better isolation at 1 GHz (-20dB) than the Semtech SC4215A Native NFET Regulator (-10dB). This decrease in the Semtech Regulator reverse isolation performance is expected due to the increased bridging capacitance and lower gm of the Native MOSFET device in the SC4215A when compared to the NPN bipolar device in the LM317 Regulator.

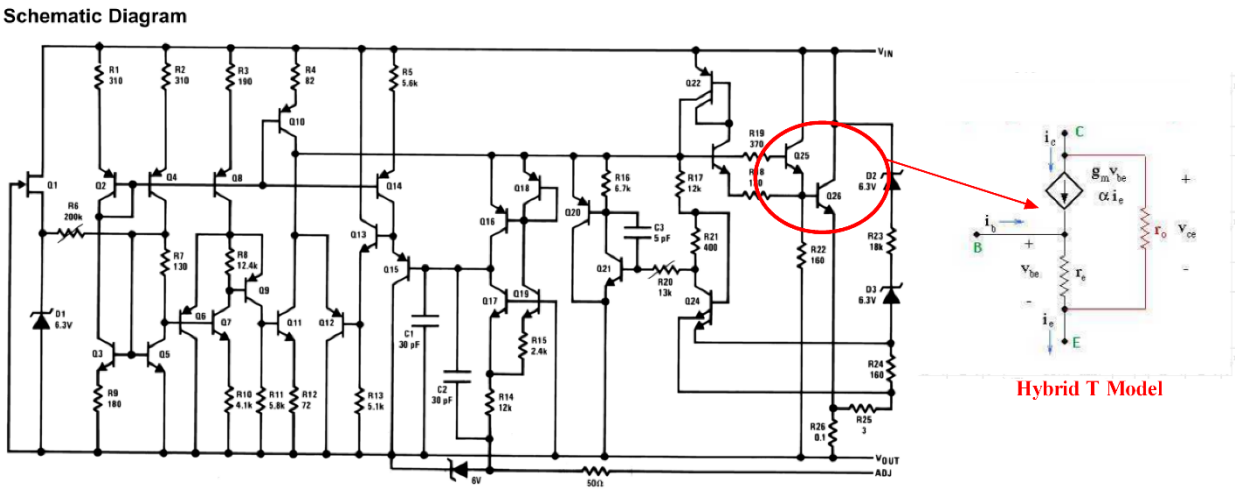


Figure 6: LM317 Series Pass Regulator

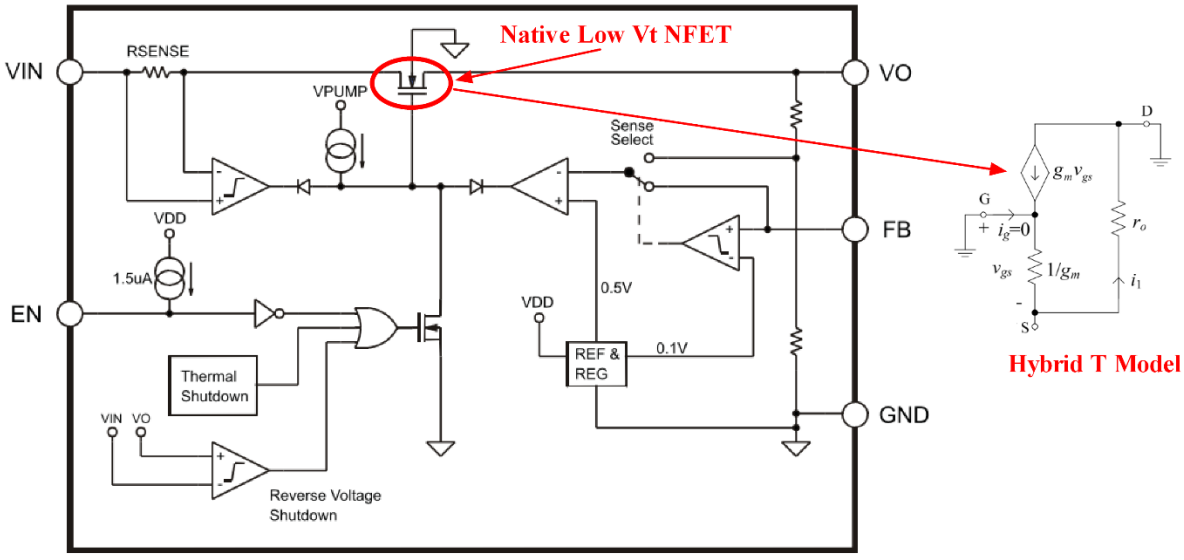


Figure 7: SemTech SC4215A Series Pass Native NFET Regulator

Figures 8, 9, and 10 show measurement results consisting of time domain supply noise and the resultant reverse coupling through the LM317 and SC4215A regulators. The noise source is a Pseudo-Random Linear Feedback Shift Register (LSFR) which produces a cyclical, repeatable noise pattern for testing. Figures 8 and 9 show the simplified top level test structures, Figure 10 shows close-ups and measurement results of the resultant input waveform when the regulator is required to supply dynamic currents to the LSFR without the aid of a reservoir capacitor. In observing the LM317/SC4215A regulator input waveform, one can clearly see much reduced frequency content on the input waveform verses what is being required of the regulator by the LSFR. Since the impedances at the input supply and output nodes of the regulators are similar, one can conclude that the inductive action of current being pulled from the series pass regulators is tracking and supplying the needed dynamic currents, leaving only small amounts of AC residuals and DC tracking currents at the regulator input supply node.

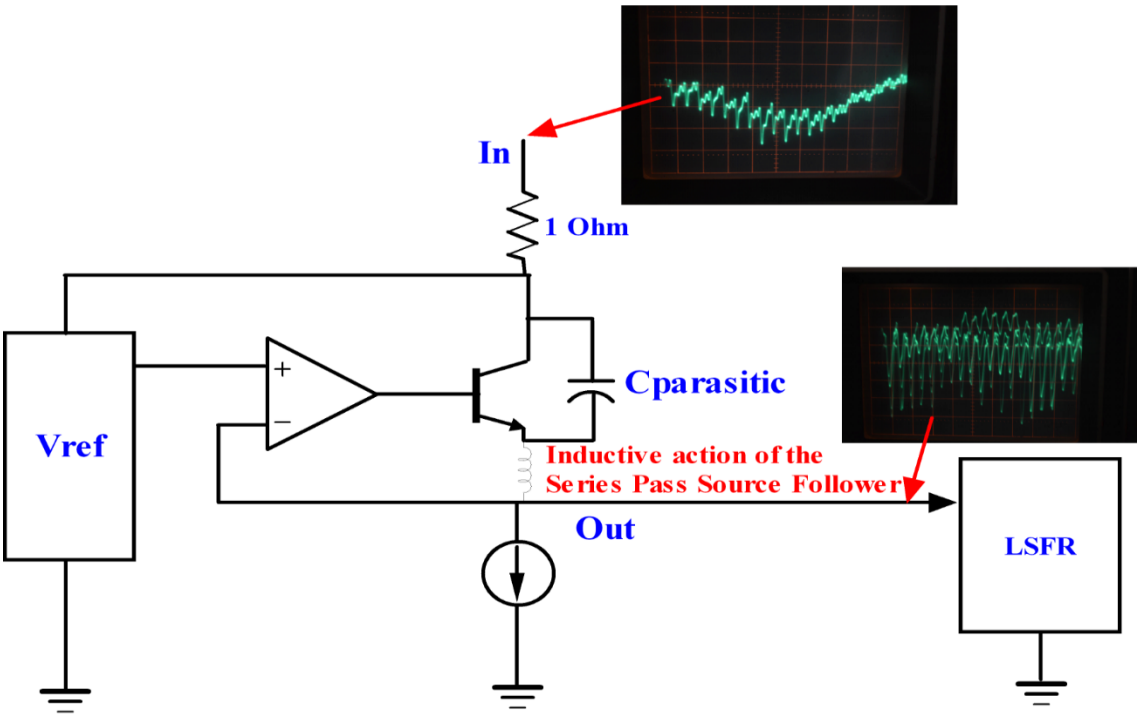


Figure 8: LM317 Series Pass Regulator Reverse Isolation Test

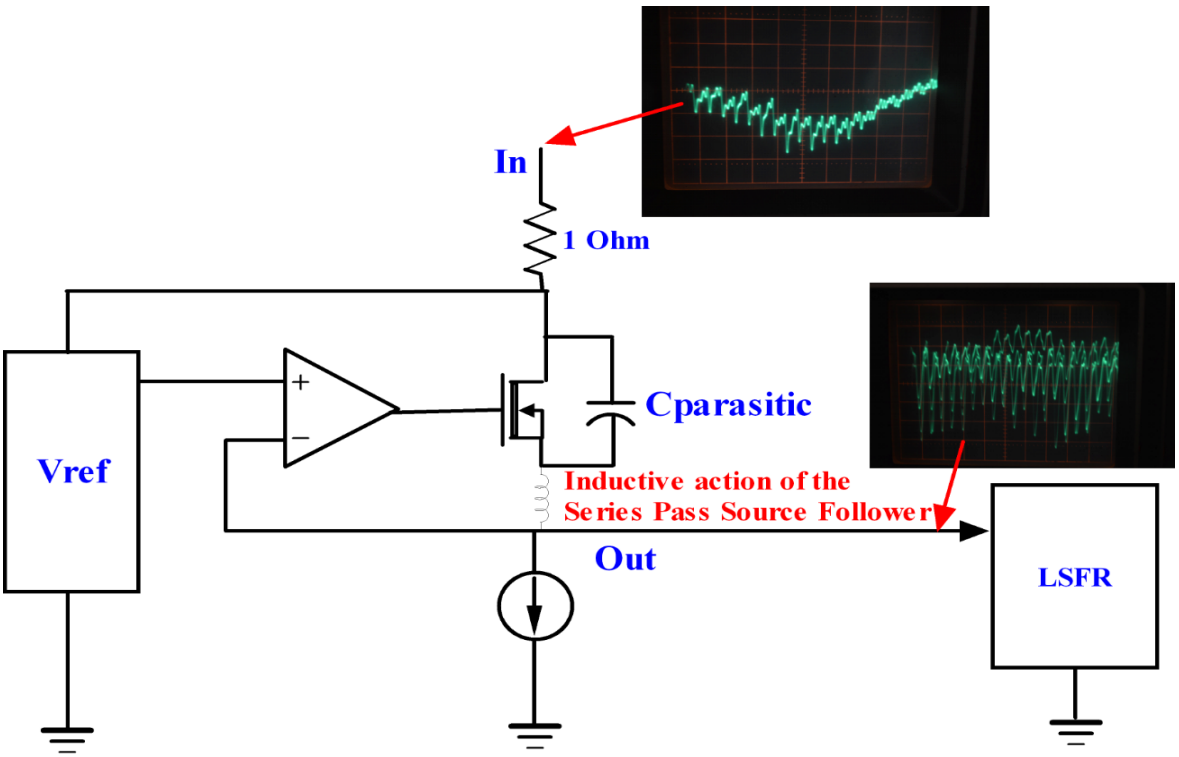
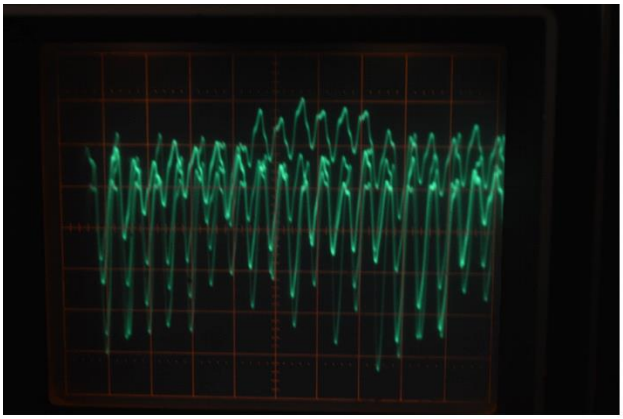
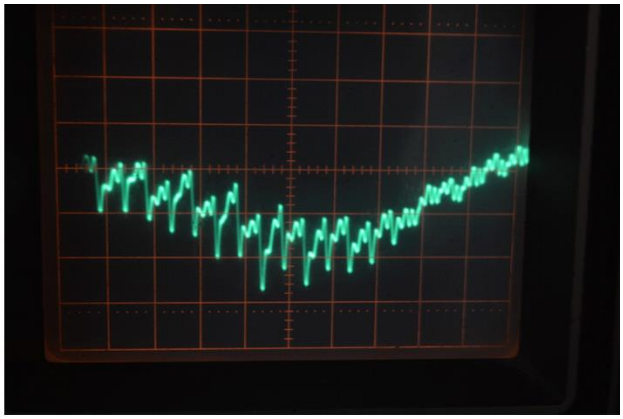


Figure 9: SC4215A Series Pass Native NFET Regulator Reverse Isolation Test



Regulator Ouptut--50mV per Division
(200mVpp Supply Noise)



Regulator Input--20mV per Division
(30mVpp max Noise Leakage)

Figure 10: Series Pass Regulator Reverse Isolation Performance

The Figure 8, 9, and 10 test shows the inherent isolation that series pass regulators provide for system internal power grids. The series pass regulator "contains" system dynamic noise and enhances the CC-100, PowerStic, and Exodus power recycling and power performance at the output node of series pass regulators.

Linear LDO Regulators

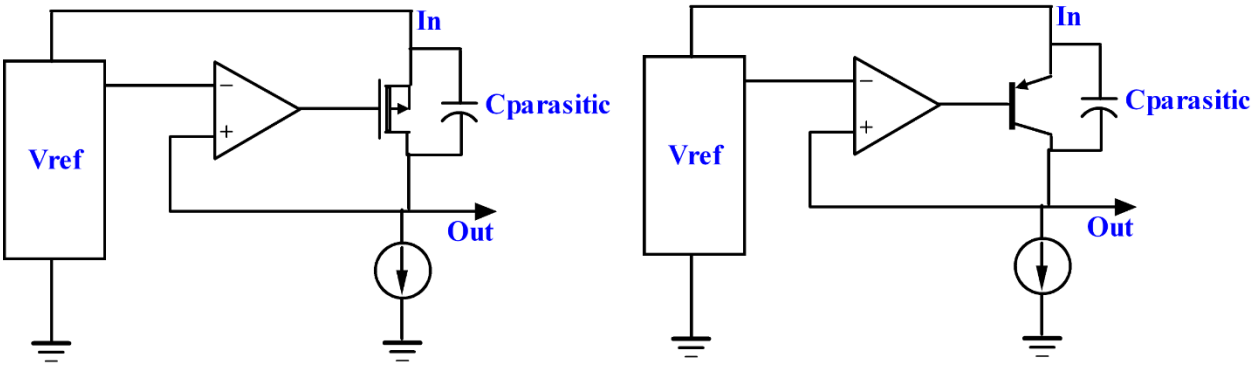


Figure 11: Linear LDO Architecture

Figure 11 shows the basic architecture of a linear low drop-out (LDO) regulator. Generally, the regulator consists of a fixed reference (Vref) and a Fet or a bipolar transistor controlled and driven by a negative feedback loop containing a high gain element (Op Amp). Usually, a current source is utilized to bias the common source element in the architecture, but can be omitted in low power applications. The Cparasitic element in the above architecture is generally ignored in most applications, but is important when considering the effects of high frequency reverse isolation in regulators

Basic Models

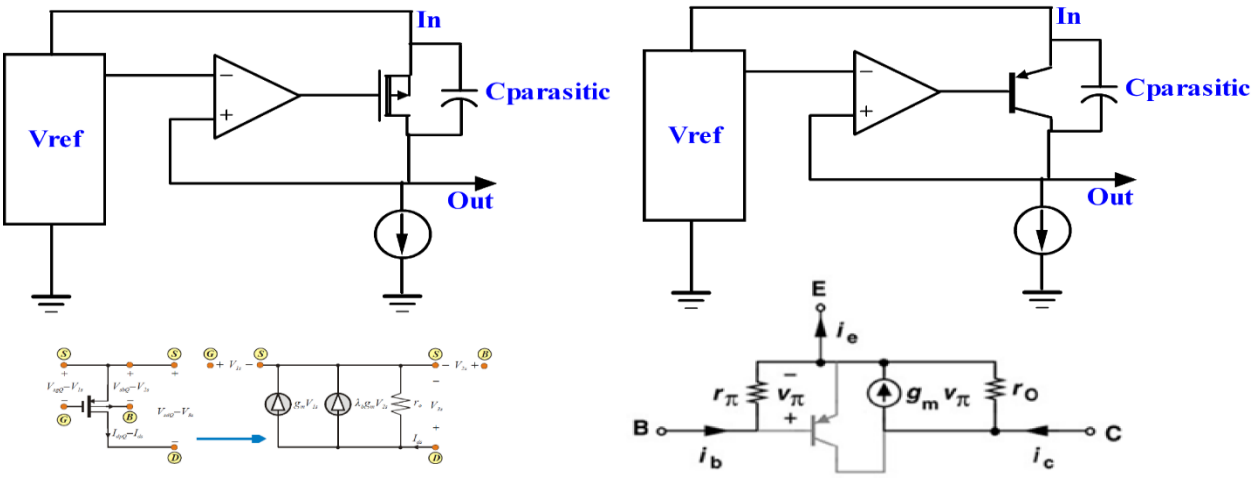


Figure 12: Linear LDO Regulator Models

The common source element in the architectures shown in Figures 11 and 12 determine the high frequency reverse isolation characteristics of the LDO regulator. Small signal hybrid pi modeling is appropriate for use here, in that the small signal dynamic characteristics of the common source transistor sets the reverse isolation performance of the regulator in this configuration. The LDO architecture does not have an inductive characteristic (see figures 12 and 13) due to the embedded common source transistor configuration. At DC or frequencies at or below the unity gain bandwidth of the control Op Amp, the control loop forces the gate/base of the common source transistor to track the events at the drain/collector, thus enabling circuit regulation. At frequencies above the unity gain bandwidth of the control Op Amp, however, the regulator control loop cannot drive the common source element in the architecture fast enough to react to the current changes demanded of the regulator, thus Cds or Cce is the only source of the needed high frequency current.

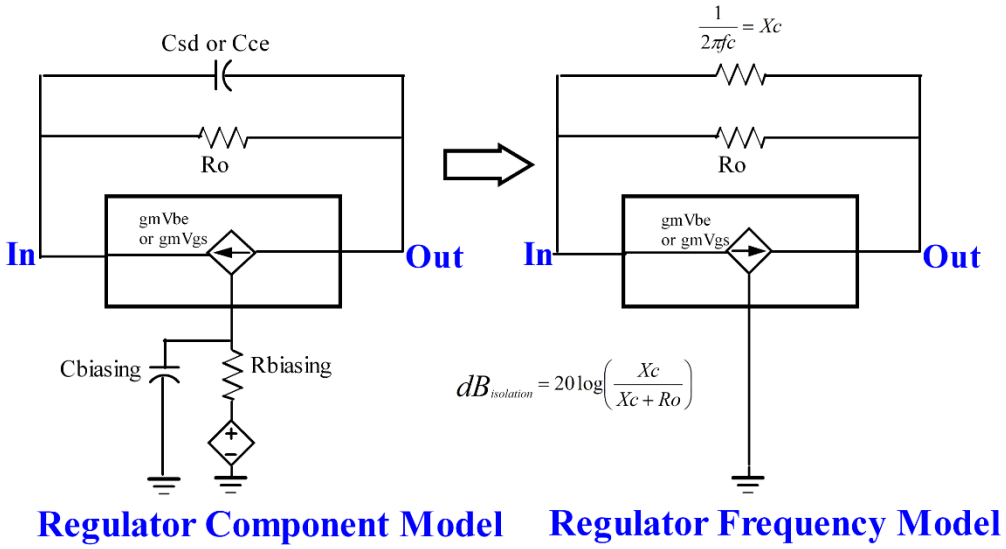
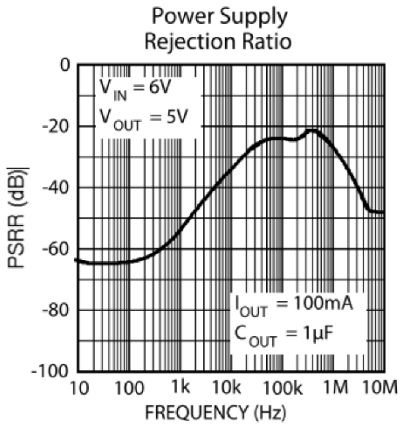


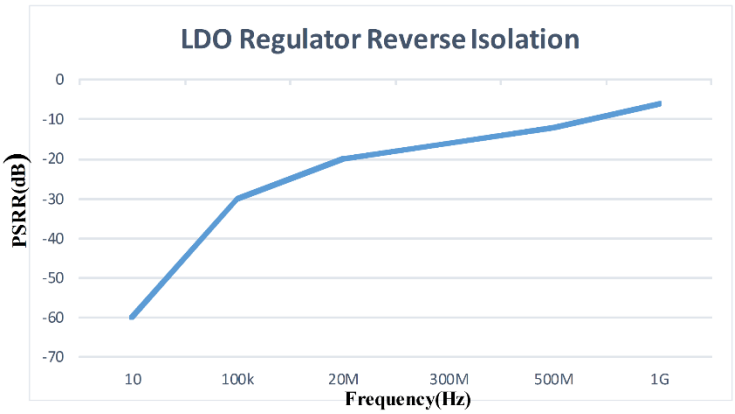
Figure 13: Linear LDO Regulator Macro Model

The simplified models of Figure 13 show the elements involved and the mathematical relationship as it relates to regulator reverse isolation. The model shown in Figure 13 shows a simple high frequency relationship between the output resistance of the series pass element (Ro) and the frequency response of the bridging capacitance (Xc), the isolation of the regulator. The resulting regulator isolation is expressed in dB.

As Xc of the bridging device increases, the reverse isolation of the regulator increases. Thus at relatively low noise frequencies, Xc, the reactance of the bridging capacitor, increases, lowering the overall conductance, forcing currents through the common source element, forcing the control loop to drive the base/gate of the common source element to deliver the needed current to the regulator load . As frequencies increase, however, the bandwidth limited control loop cannot respond fast enough to drive the circuit common source element, Xc is seen to decrease, increasing the bridging capacitance conductance, the effect being the lowering the overall regulator reverse isolation. As frequencies increase further, the Xc of the bridging capacitance becomes low enough so as to compete with the output resistance, Ro, of the common source device, thus further decreasing the reverse isolation of the regulator. This “break point” can only be adjusted by either increasing or lowering the bridging capacitance value or increasing the control loop bandwidth. The LDO has no effective inductive

reactance, thus allowing high frequency dynamic current demands to be drawn through the bridging capacitance from the regulator supply input.





Micrel LDO Regulator PSRR

Micrel LDO Regulator Measured Reverse Isolation

Figure 14: Micrel MIC5219 PSRR and Reverse Isolation

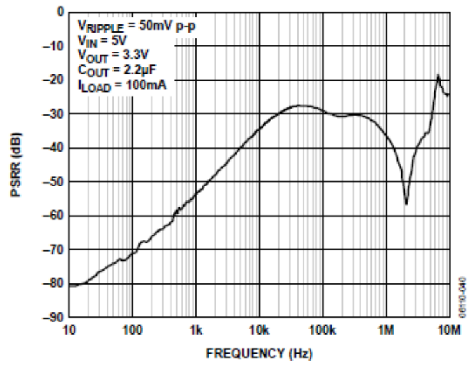
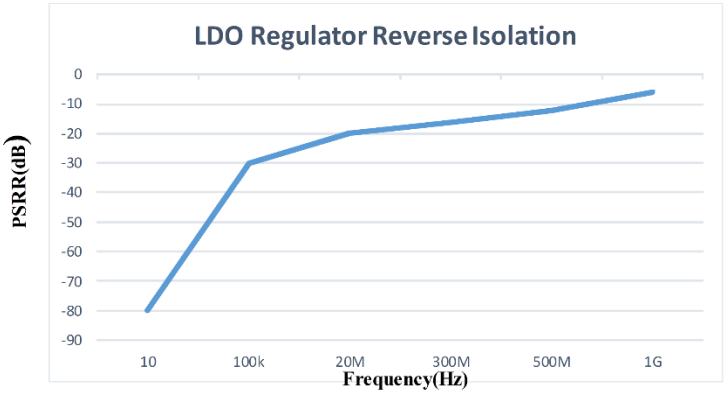


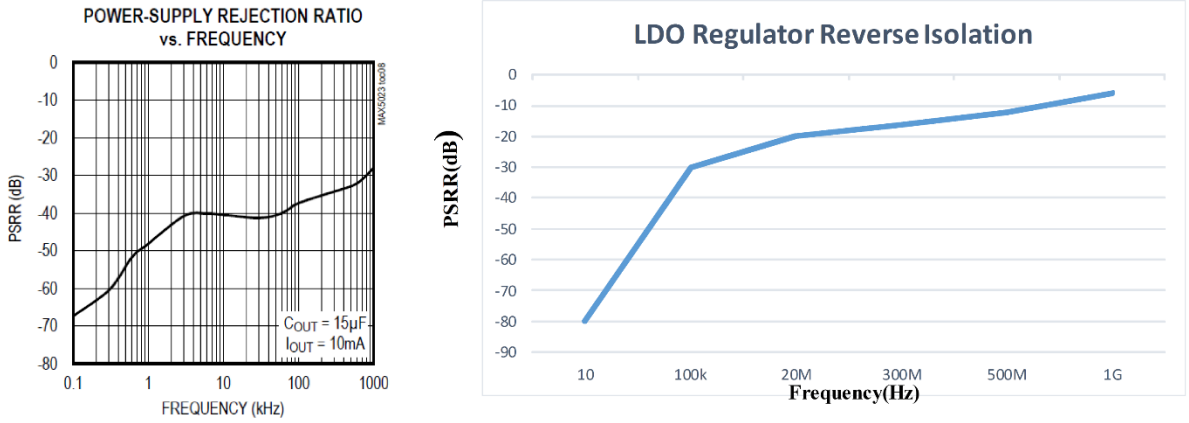
Figure 25. Power Supply Rejection Ratio vs. Frequency



ADI LDO Regulator PSRR

ADI LDO Regulator Measured Reverse Isolation

Figure 15: ADI ADP1715 PSRR and Reverse Isolation



Maxim LDO Regulator PSRR

Maxim LDO Regulator Measured Reverse Isolation

Figure 16: Maxim MAX5024L PSRR and Reverse Isolation

These coupling effects are graphically displayed in in Figures 14, 15, and 16. Three LDO regulators, the Micrel MIC5219, ADI ADP1715, and Maxim MAX5024L (schematics and block diagrams shown in Figures 17, 18, and 19) are shown to have excellent PSRR (reverse isolation) out to about 1 MHz. The PSRR/Reverse Isolation starts to degrade at frequencies greater than 1 MHz, ranging between -30dB at 1 MHz to -5dB at 1 GHz.

This decrease in regulator reverse isolation performance is expected due to the decreased bridging capacitance reactance, Xc, the limited bandwidth of the control loop, and the lack of an inductive blocking element in the LDO architecture.

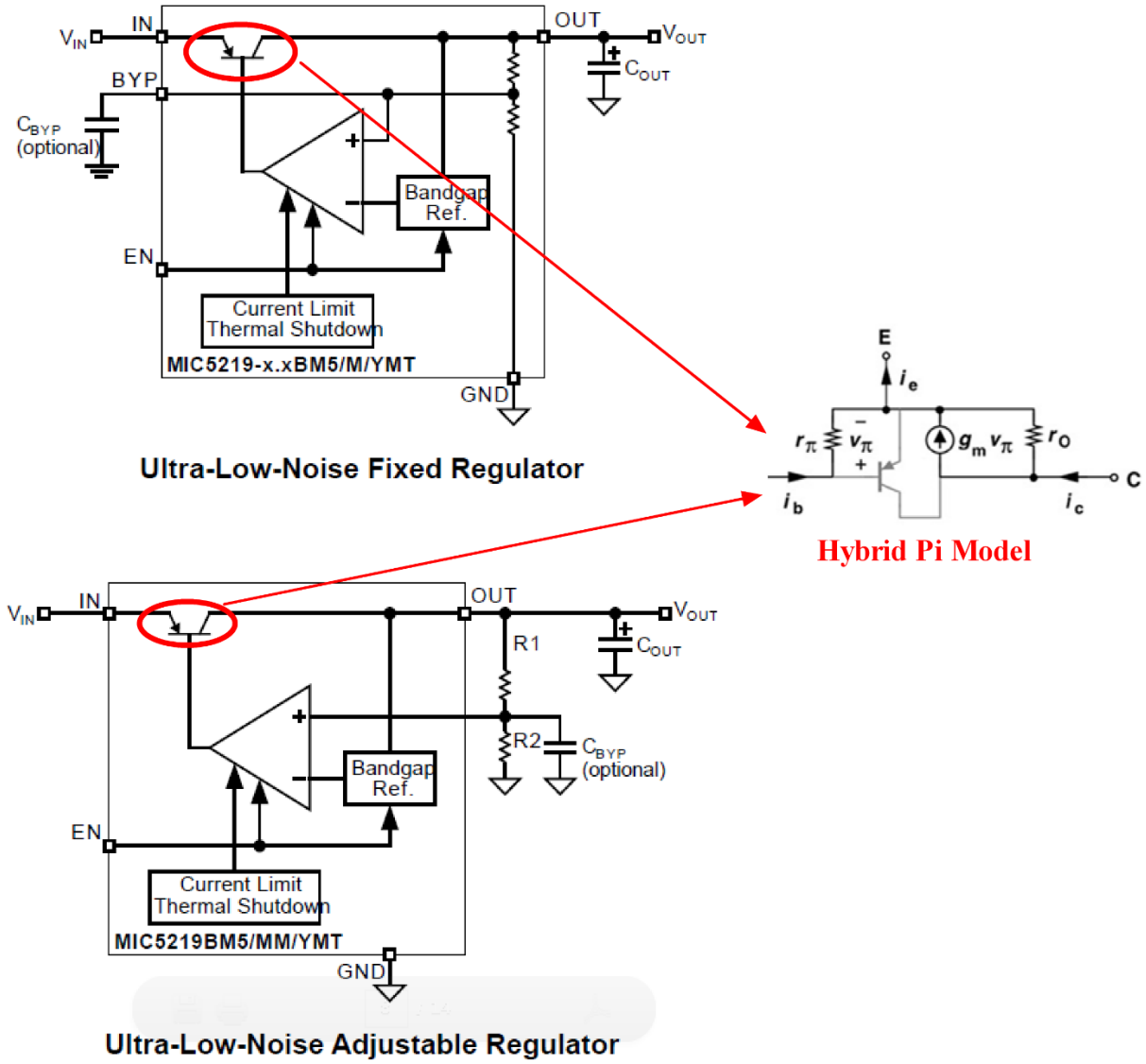


Figure 17: Micrel MIC5219 LDO Regulator

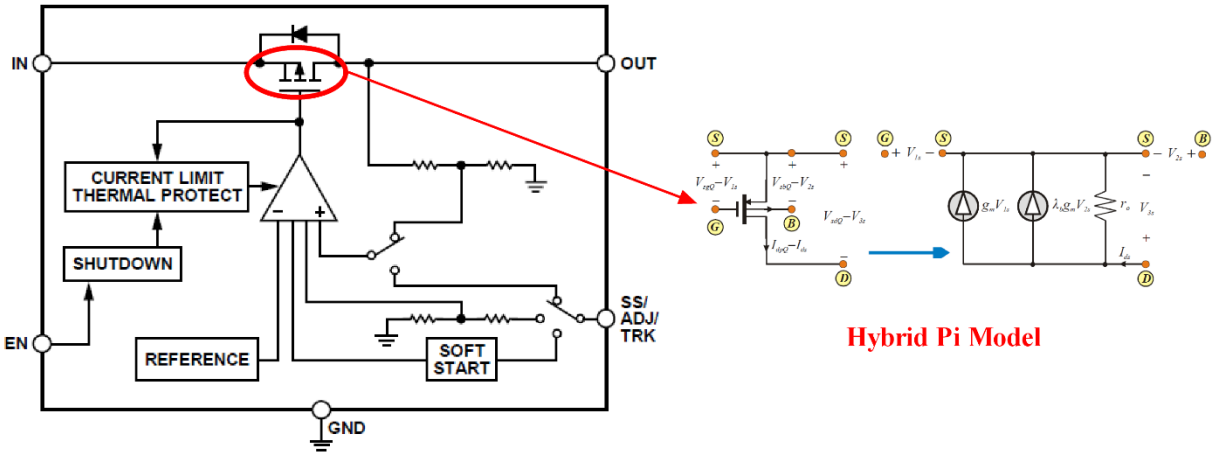


Figure 18: ADI ADP1715 LDO Regulator

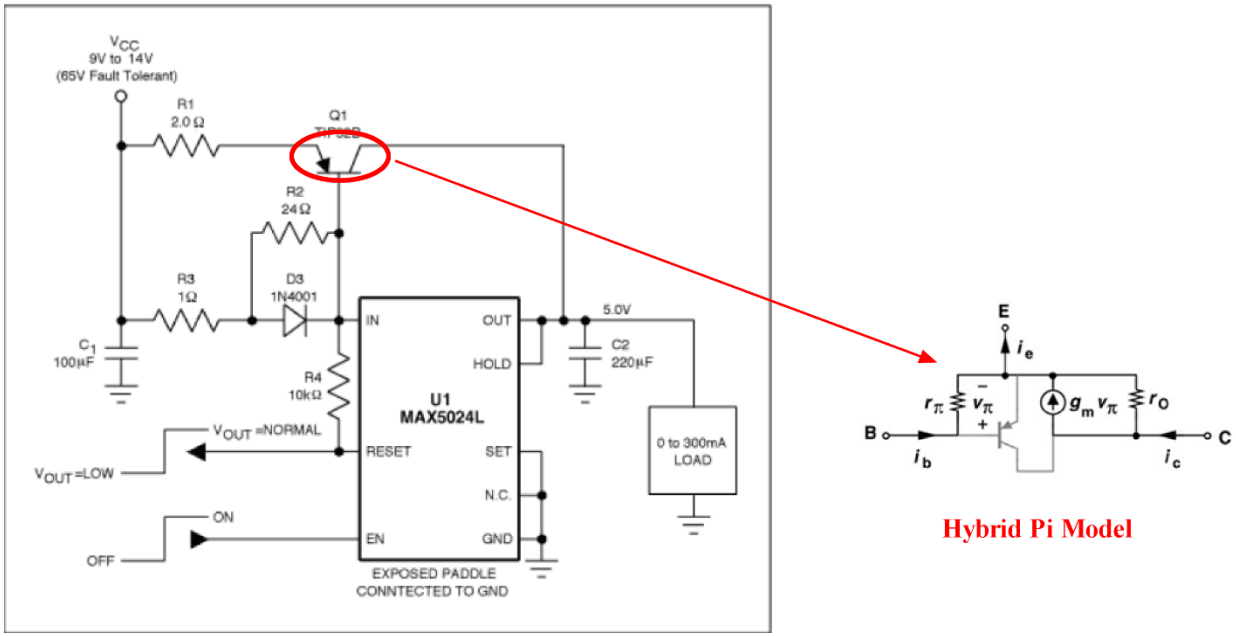


Figure 19: Maxim MAX5024L LDO Regulator

Figures 20, 21, and 22 show measurement results consisting of time domain supply noise and the resultant reverse coupling through the Micrel, ADI, and Maxim regulators. The noise source is a Pseudo-random Linear Feedback Shift Register (LSFR) which produces a cyclical, repeatable noise pattern for testing. Figures 20 and 21 show the simplified top level test structures, Figure 22 shows close-ups and measurement results of the resultant input waveform when the

regulator is required to supply dynamic currents generated by the LSFR, without the aid of an output reservoir capacitor. In observing the Micrel, ADI, and Maxim regulator input waveforms, one can clearly see a much higher magnitude and frequency content on the LDO input waveforms verses that of the LM317/Semtech regulators shown in Figure 10. Since the impedances at the input and output supply nodes of the regulators are similar, one can conclude that the high frequency dynamic currents required of the LDO cannot be obtained via the regulator circuit or common source element in the regulator, but are being drawn through the bridging capacitance around the LDO.

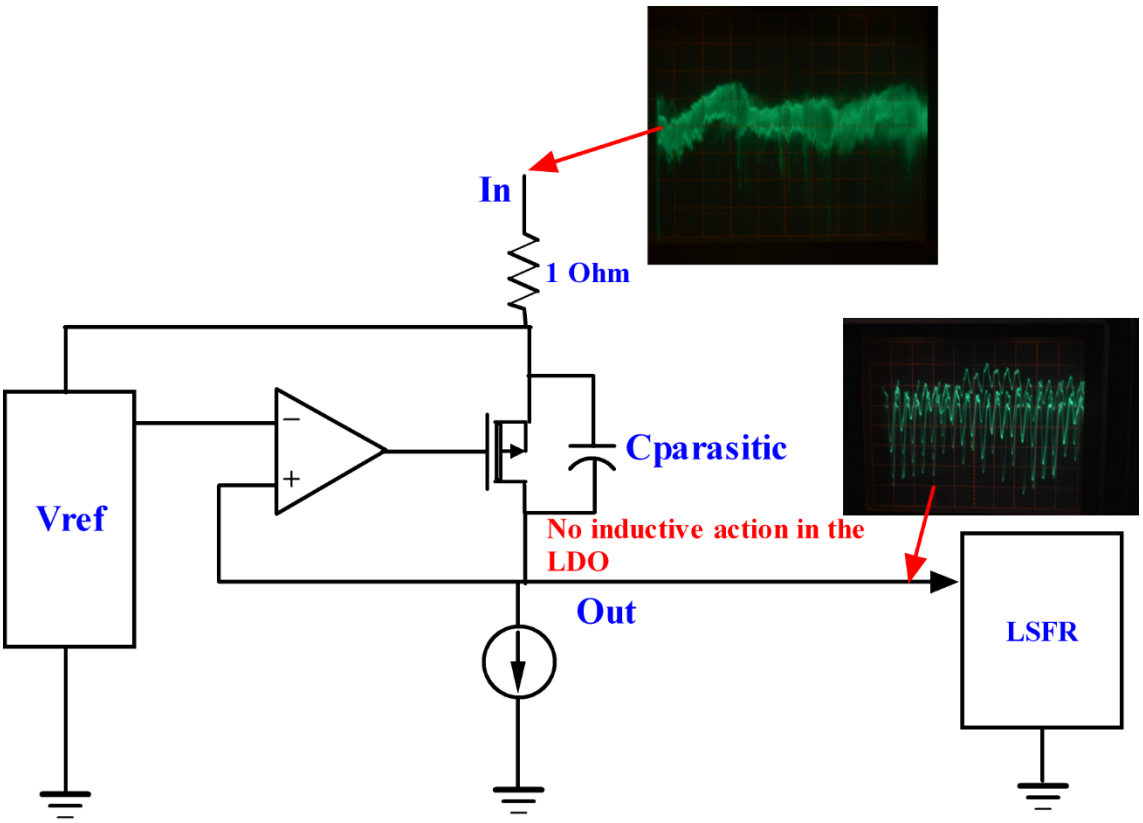


Figure 20: PMOS LDO Reverse Isolation Test

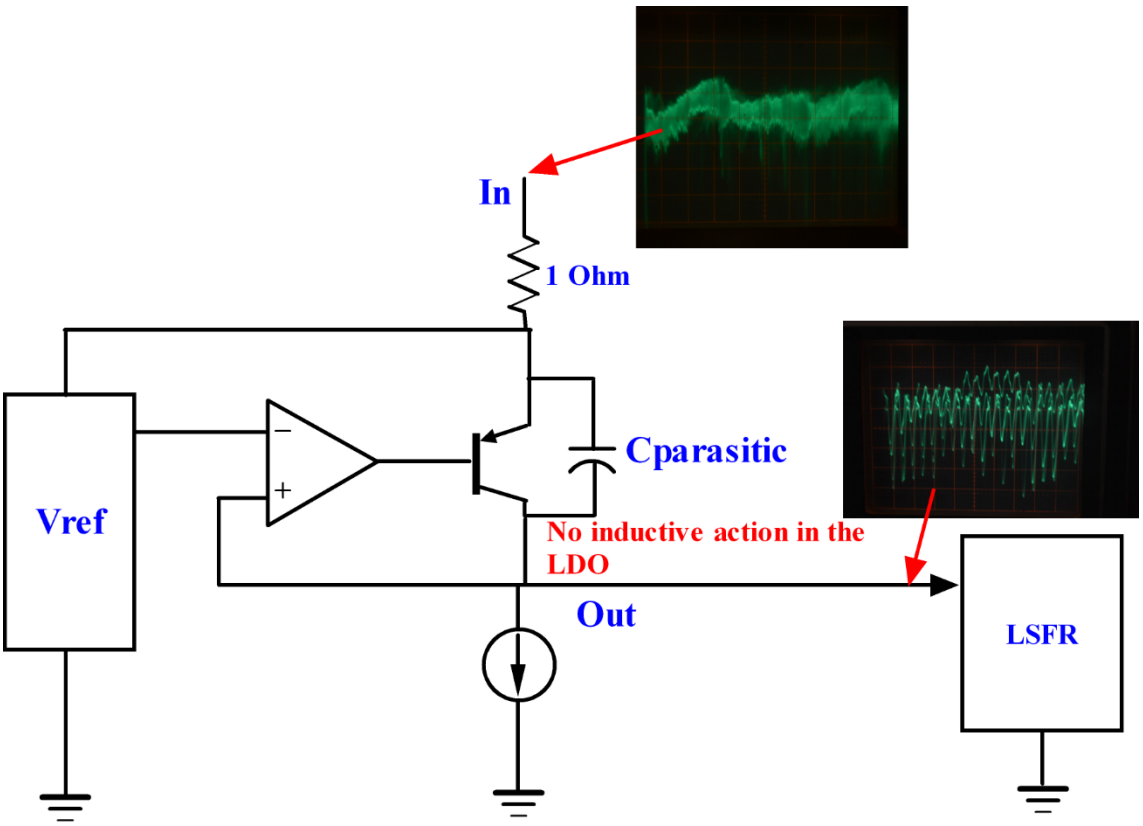
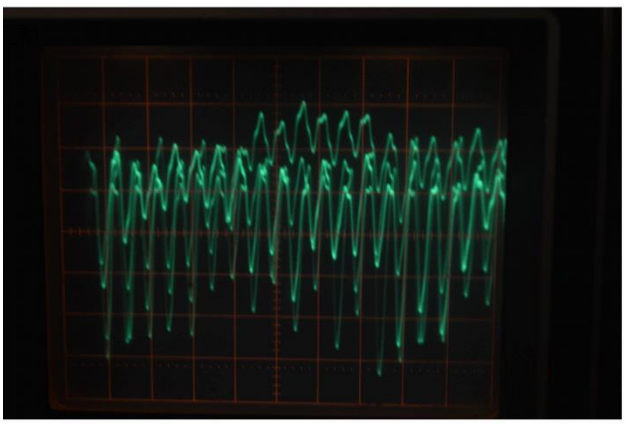
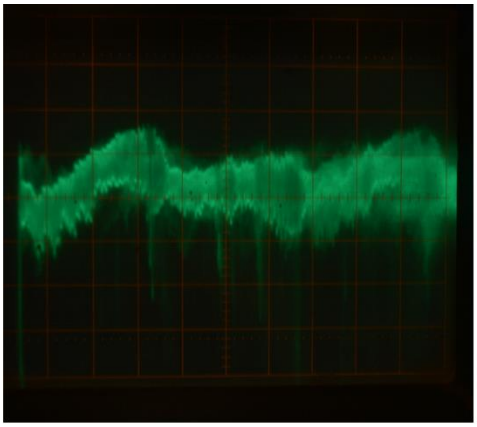


Figure 21: PNP LDO Reverse Isolation Test



Regulator Ouptut--50mV per Division (200mVpp Supply Noise)



Regulator Input--50mV per Division (100mVpp Average Noise--250mVpp High Frequency Glitches)

Figure 22: LDO Reverse Isolation Performance

The Figure 20, 21, and 22 test shows the inherently poor high frequency isolation that LDO regulators provide for system internal power grids. The LDO regulator "passes" system high frequency dynamic noise around the LDO to the output of the preceding regulator. This action explains how and why the PowerStic and Exodus devices recycle and reduce power in systems with USB ports, even if the circuit noise is not generated on the 5V USB supply.

Switch Mode Buck Regulators

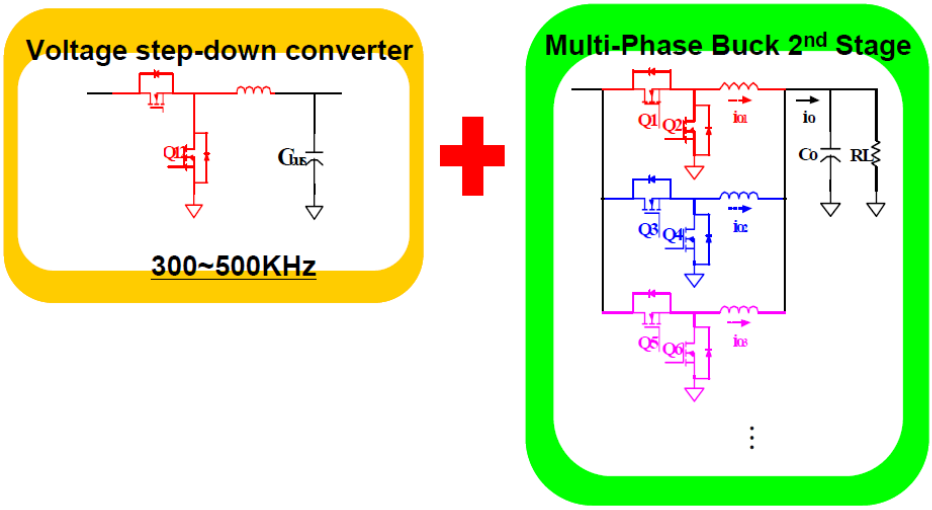


Figure 23: Typical Buck Switching Regulators

Figure 23 shows the basic topology of a switch mode Buck Converter/Regulator. A Buck Converter is a "step down" device, taking in an input high voltage and current (power), converting the input power to a lower output voltage with a "step up" in current. Buck converters are utilized for their high efficiency in this down conversion function, and usually achieve Power In/Power Out efficiencies greater than 90%.

The Buck converter generally consists of a high power storage inductor (see Figure 24 for characteristics), an output filtering cap, a Mosfet, source connected to ground on the input of the power inductor, utilized for inductor grounding during the flyback phase of operation, and a Mosfet connected in series with the input supply, which activates during the power inductor charging or boost phase of operation.

Not much is published on the effects of high frequency noise at the output of the converter coupling back to the input of the converter and the preceding input stage, known as high frequency reverse isolation.

Features

- Available in E6 series
- Unit height of 3.8 mm
- Current up to 7.2 A
- RoHS compliant*

Applications

- Input/output of DC/DC converters
- Power supplies for:
  - Portable communication equipment
  - Camcorders
  - LCD TVs
  - Car radios

SRU1038 Series - Shielded SMD Power Inductors

Electrical Specifications

Bourns Part No.	Inductance 100 KHz (µH)	Tol. %	Q Ref.	Test Freq. (MHz)	SRF Typ. (MHz)	RDC (mΩ)	Irms Max. (A)	Isat Typ. (A)	**K-Factor
SRU1038-1R5Y	1.5	±30	14	7.96	65.0	5.2	7.20	7.00	177
SRU1038-2R2Y	2.2	±30	12	7.96	55.0	7.7	6.80	6.50	145
SRU1038-2R5Y	2.5	±30	12	7.96	50.0	12.5	6.10	6.00	136
SRU1038-3R5Y	3.5	±30	14	7.96	24.0	11.5	5.50	5.50	106
SRU1038-3R8Y	3.8	±30	14	7.96	35.0	15.0	5.50	5.50	104
SRU1038-5R0Y	5.0	±30	12	7.96	30.0	14.5	4.60	4.80	94
SRU1038-5R2Y	5.2	±30	12	7.96	30.0	22.0	4.60	4.80	92
SRU1038-6R2Y	6.2	±30	12	7.96	25.0	16.5	4.00	4.20	84
SRU1038-6R8Y	6.8	±30	13	7.96	36.0	35.0	3.90	4.00	80
SRU1038-8R2Y	8.2	±30	12	7.96	22.0	32.0	3.80	3.90	73
SRU1038-100Y	10.0	±30	24	7.96	20.0	25.0	3.80	3.60	64
SRU1038-150Y	15.0	±30	24	2.52	16.0	37.0	2.80	2.70	51
SRU1038-220Y	22.0	±30	20	2.52	12.0	55.8	2.20	2.30	43
SRU1038-270Y	27.0	±30	22	2.52	11.0	78.0	1.85	1.90	39
SRU1038-330Y	33.0	±30	22	2.52	10.0	86.0	1.80	1.80	35
SRU1038-470Y	47.0	±30	22	2.52	8.0	121.0	1.65	1.60	29
SRU1038-680Y	68.0	±30	24	2.52	7.0	166.0	1.10	1.30	26
SRU1038-101Y	100.0	±30	24	0.796	6.0	220.0	1.30	1.10	20
SRU1038-151Y	150.0	±30	20	0.796	5.0	358.0	0.90	0.80	16
SRU1038-221Y	220.0	±30	22	0.796	4.0	565.0	0.65	0.65	14
SRU1038-331Y	330.0	±30	20	0.796	3.0	773.0	0.55	0.52	11

**K-Factor: To calculate core flux density, Bp-p (gauss) = K x L(µH) x Δ I (peak-to-peak ripple current, A), determine core loss from *Core Loss vs. Flux Density* plot on page 2.

General Specifications

Test Voltage ..... 1 V
Reflow Soldering .. 230 °C, 50 sec. max.
Operating Temperature
..... -40 °C to +125 °C
(Temperature rise included)
Storage Temperature
..... -40 °C to +125 °C
Rated Current
..... Ind. drop 35 % typ. at Isat
Temperature Rise
..... 40 °C max. at rated Irms
Resistance to Soldering Heat
..... 260 °C for 10 sec.

Materials

Core ..... Ferrite DR and RI core
Wire ..... Enameled copper
Terminal ..... Ag/Ni/Sn
Packaging ..... 800 pcs. per reel

Product Dimensions

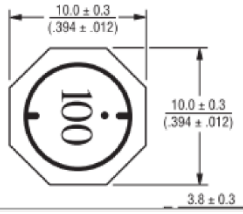


Figure 24: Buck Switching Inductor Characteristics

Figure 25 shows the basic Buck converter components and their important parasitic components. One will notice in Figure 25 and the table in Figure 24, that power inductors tend to have relatively high inductance values (uH), low self-resonant frequencies, therefore, high inter-winding capacitances. Assuming sufficient magnitude high frequency, dynamically generated, load noise, and also assuming a relatively low Q filter capacitor at the Buck Converter output, the inter-winding power inductor capacitance is high enough in value (about 8pF with the highlighted 47uH inductor of Figure 24) to provide a pass through capacitance for this noise back to the converter input.

The simplified models of Figure 25 show the converter in its boost or charging phase, with the Mosfets switched to their appropriate states, providing a low impedance path for high frequency noise passing through the power inductor, blocked by an approximated 100nh of trace inductance of the flyback path, forcing noise currents through the "on" input power Mosfet. This path on the right hand side of Figure 25 reduces to essentially a low series Mosfet channel resistance and the inter-winding power inductor capacitance.

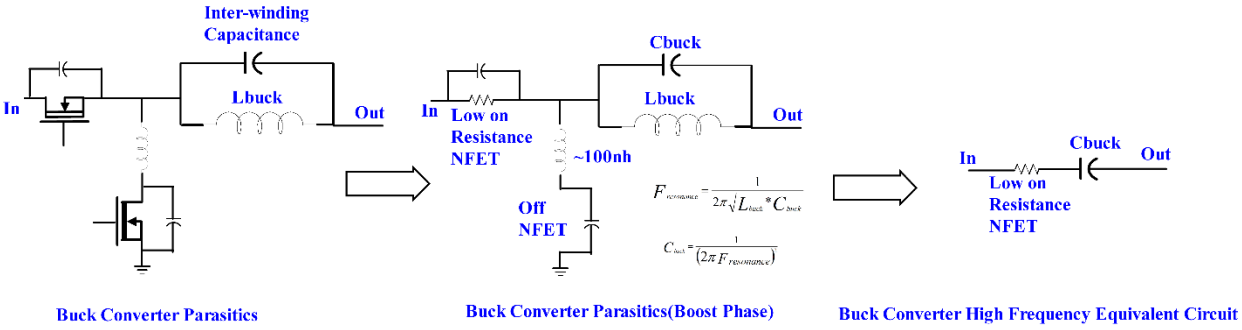
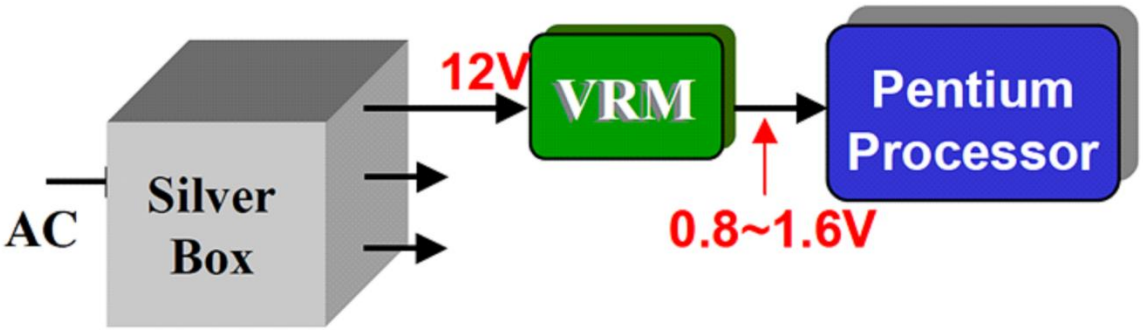
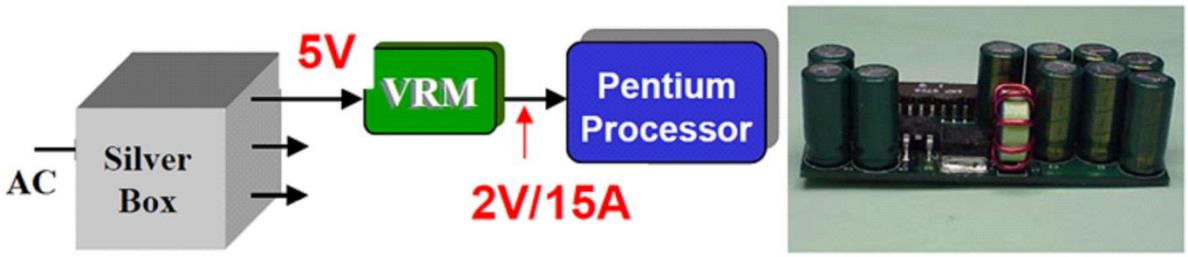


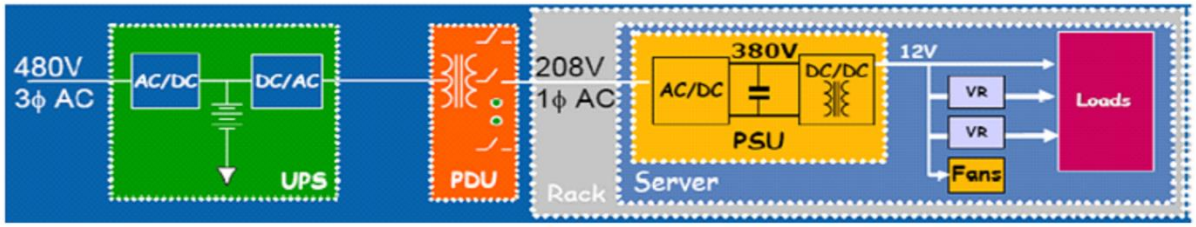
Figure 25: Buck Switching Regulator Macro Models

As Figure 25 depicts, the Buck Converter in the boost or changing phase, reduces to a simple low R, moderate C coupling circuit for high frequency load noise.

Applications in Switching and Logic Circuit Systems







Computer and Server Power Architectures

Figure 26: Common Computer and Server Architectures

Figure 26 shows common power distribution regulator networks used in computing and server devices. The VRM and VR elements in the Figure 26 diagrams can be Linear Series Pass, LDO, or Non-linear Switch Mode Buck Regulators.

Figure 27 shows the potential reverse coupling through each network described in Figure 26, assuming sufficient digital activity and that LDOs and/or Switching Buck Regulators are utilized.

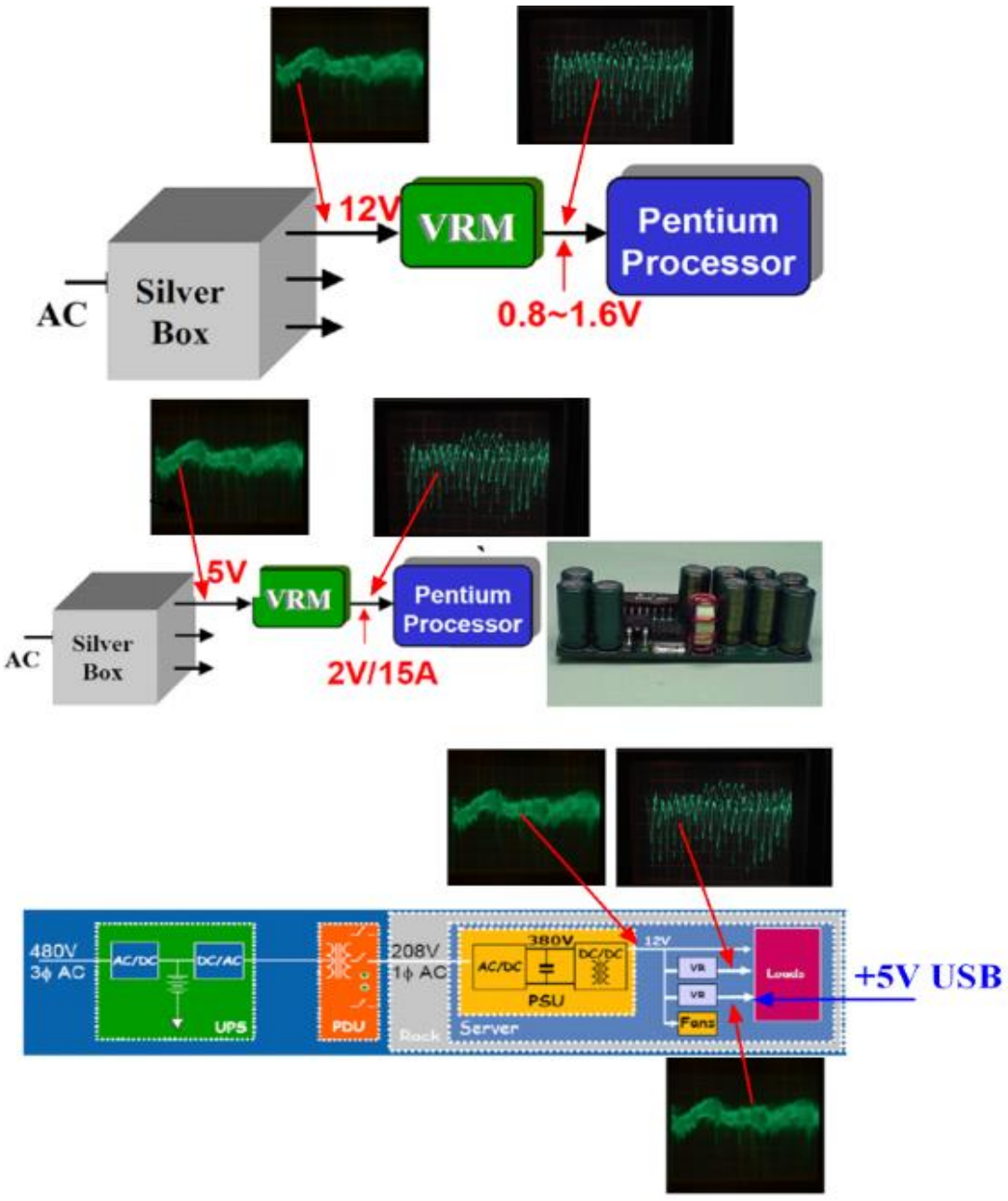


Figure 27: Potential Coupling in Computer and Server Architectures

The top and middle diagrams in Figure 27 shows the reverse coupling present if LDOs and/or Switching Buck Regulators are utilized, the lower diagram (server example) in Figure 27 shows the potential coupling path from the system processor, reverse coupling through the supply regulator to the +12V system

supply, then forward through the +5V USB supply regulator. These coupling scenarios are the energy source and paths responsible for the CurrentRF PowerStic and Exodus devices system power reduction performance.

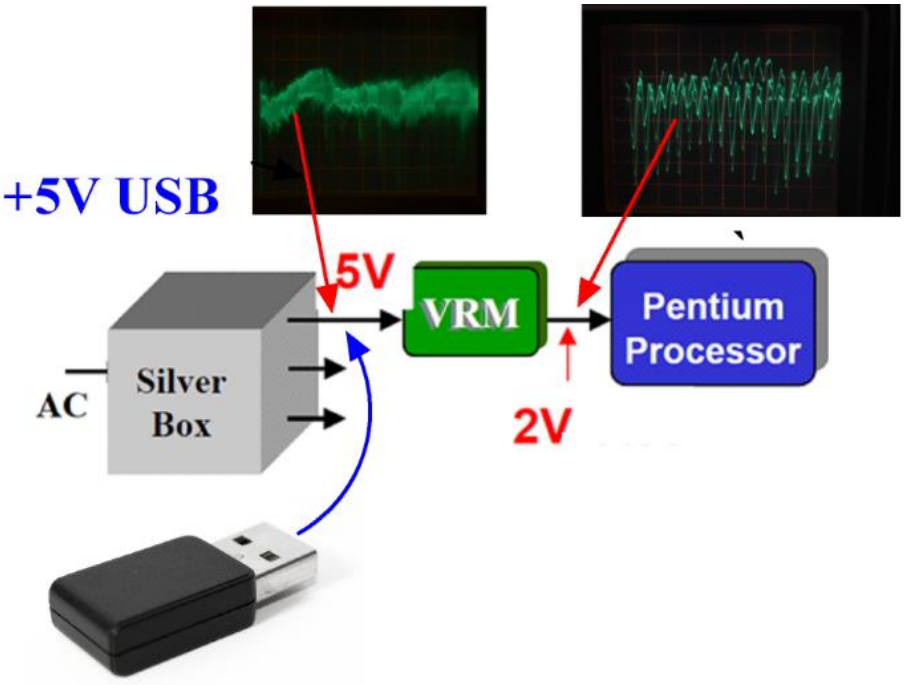
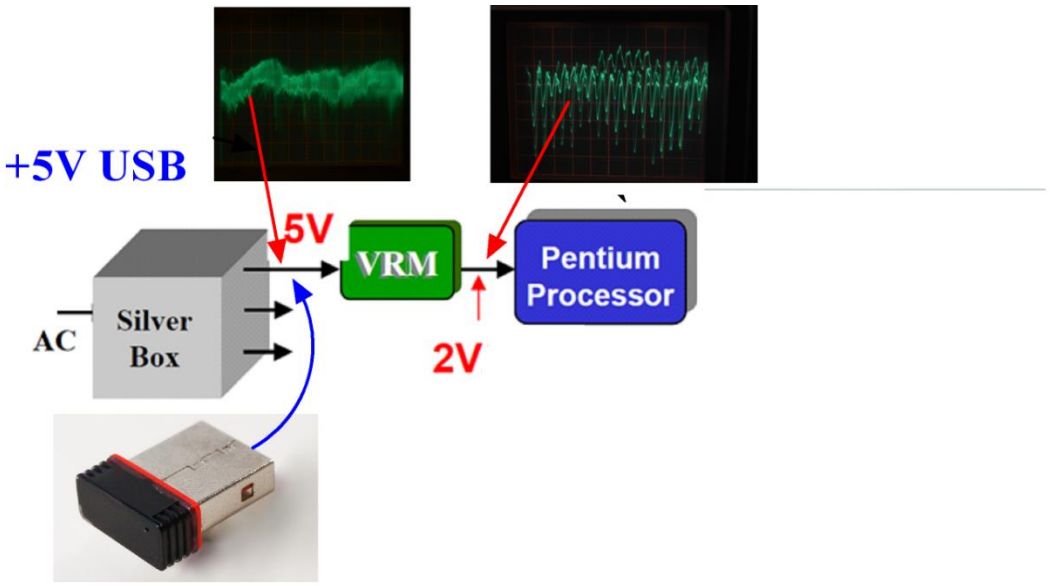


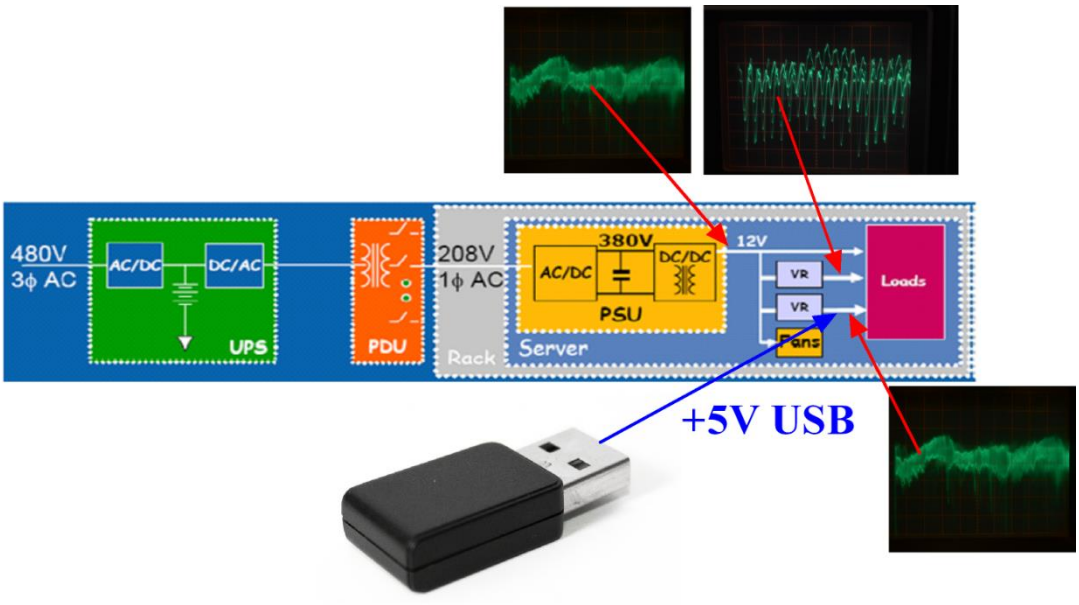
Figure 28: Coupling Paths in Portable Computing Devices



Exodus System Model

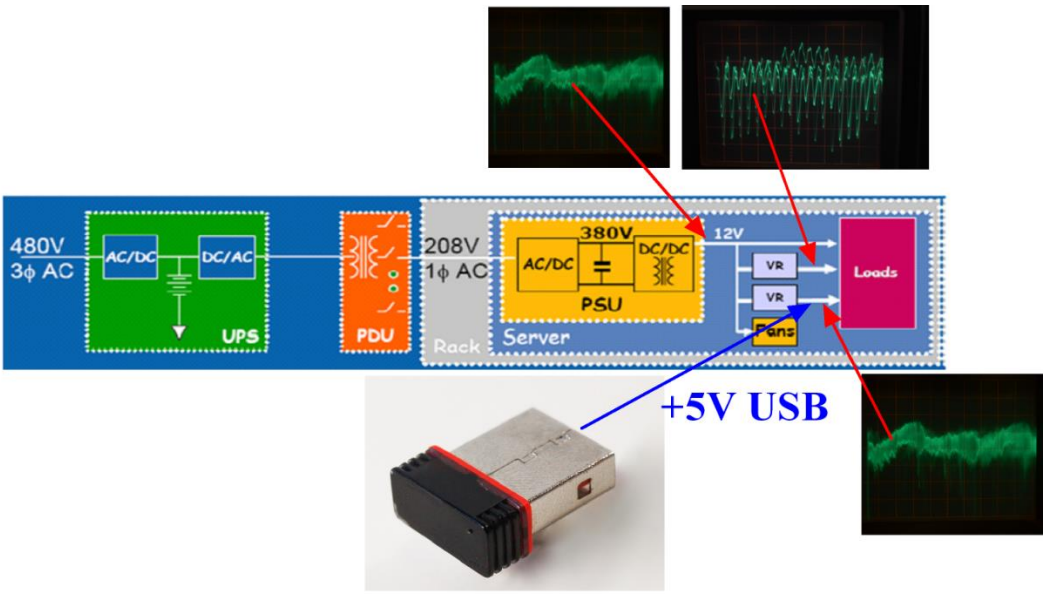
Figure 29: Coupling Paths in Portable Computing Devices

Figures 28 and 29 show a typical PowerStic and Exodus portable device system coupling model in which LDOs and or Switching Buck Regulators are utilized. Examining the diagrams, one can see the reverse coupling through the onboard regulators, this coupling producing the resultant high frequency energy for the PowerStic and Exodus devices, allowing them to recycle this energy back into the system for power reduction.



PowerStic System Model

Figure 30: Coupling Paths in Network and Server Devices



Exodus System Model

Figure 31: Coupling Paths in Network and Server Devices

Figures 30 and 31 shows a typical PowerStic and Exodus network and server system reverse/forward system coupling model in which LDOs and or Switching Buck Regulators are utilized. Examining the diagrams, one can see the reverse coupling path from the system processor, reverse coupling through the supply regulator to the +12V system supply, then forward through the +5V USB supply regulator. This coupling is responsible for resultant high frequency energy for the PowerStic and Exodus devices, allowing them to recycle this energy back into the system for power reduction

USB Memory Sticks and Peripherals

USB data transfers and activity provide a rich source of energy for PowerStic and Exodus energy harvesting and power reduction. The diagrams in Figures 32 and 33 shows a typical USB peripheral architectures. The Silicon Labs C8051F38x in Figure 32 contains an LDO, powered by the native +5V USB supply, the LDO supplying power for the onboard CPU, Memory, the 48Mhz Oscillator, and the USB function controller. The CMOS activity associated with the function of the peripheral, coupled through the onboard LDO, provides a rich source of high frequency energy for the PowerStic and Exodus devices to harvest.

The FTDI Host controller in Figure 33 spells out the voltage regulator structure typically utilized in most USB Host controllers, Mixed Signal, and Digital Chips. LDOs are utilized for low power and low headroom performance, and effectively couple high frequency digital currents to the PowerStic and Exodus devices, enabling thier power reduction performance.

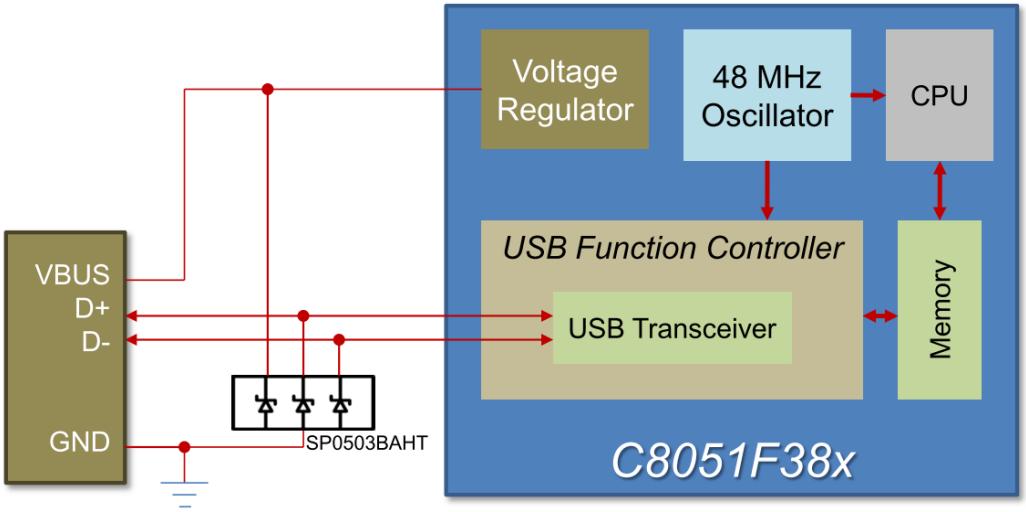


Figure 32: Silicon Labs USB Host Controller

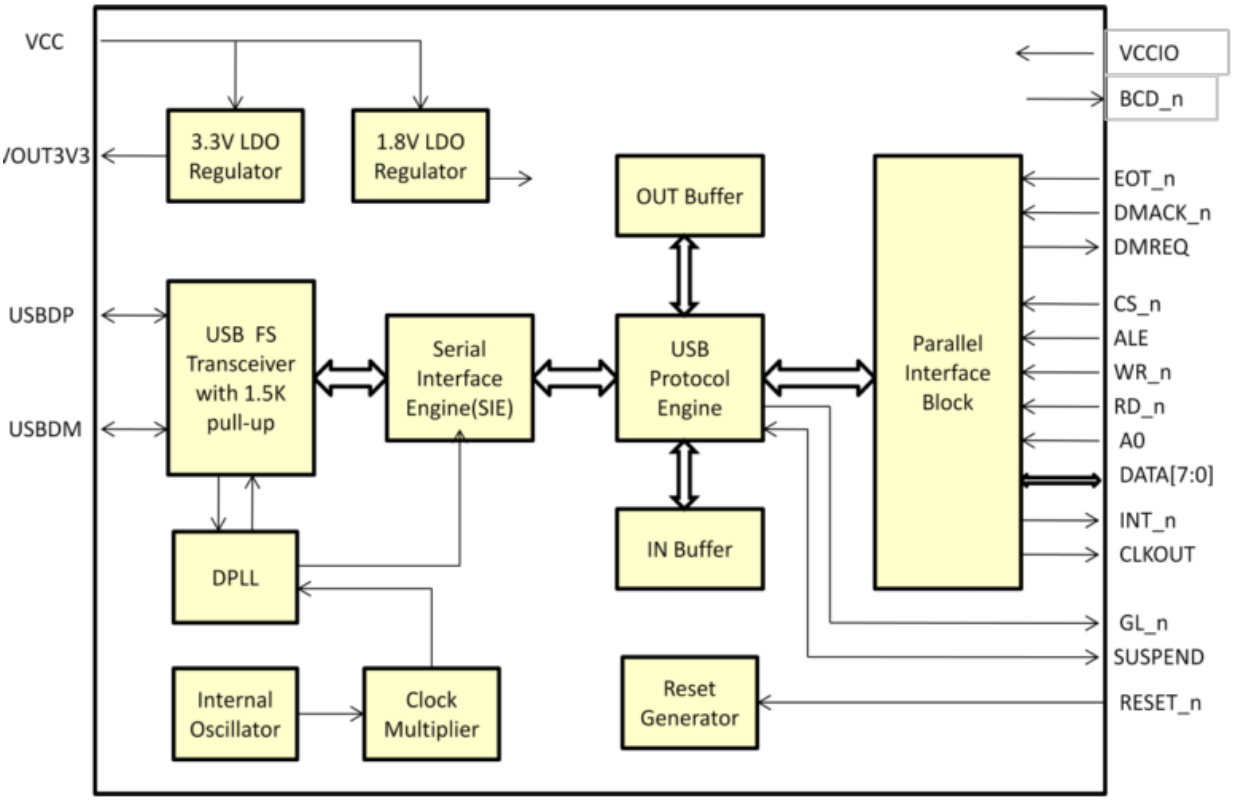


Figure 33: FTDI USB Host Controller

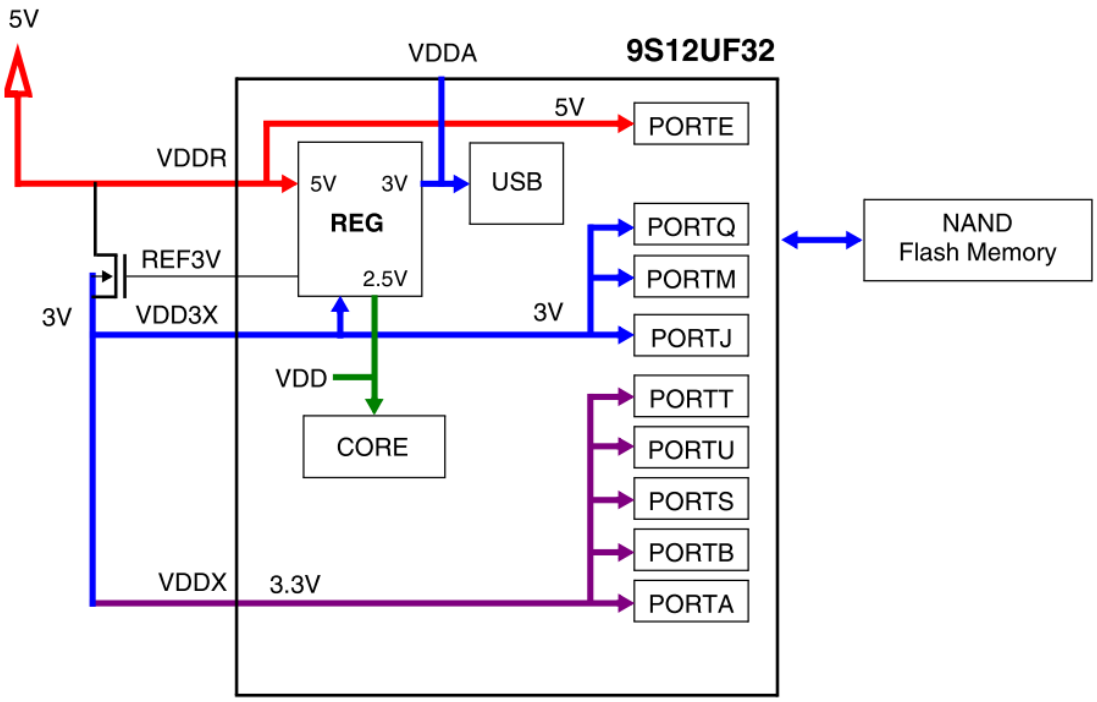


Figure 34: Freescale Flashdrive Controller

Figure 34 shows the internal structure of the Freescale 9S12UF32 Flashdrive Controller used in many Memory Stick Flashdrives. Examining Figure 34, one can recognize both LDOs (the 2.5V and 3V internal supplies) and a series pass regulator (the 3.3V supply).

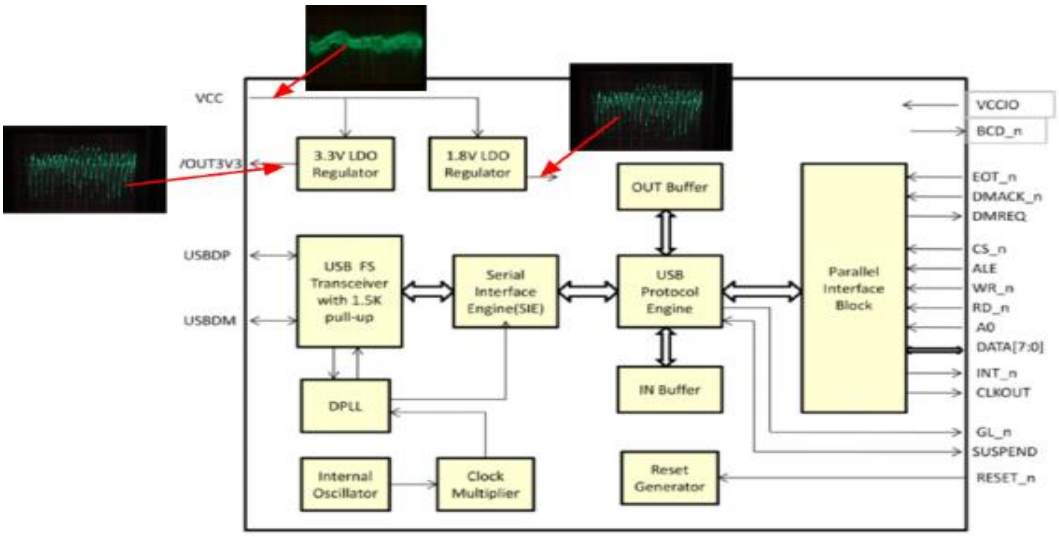


Figure 35: FTDI USB Host Controller Reverse Coupling

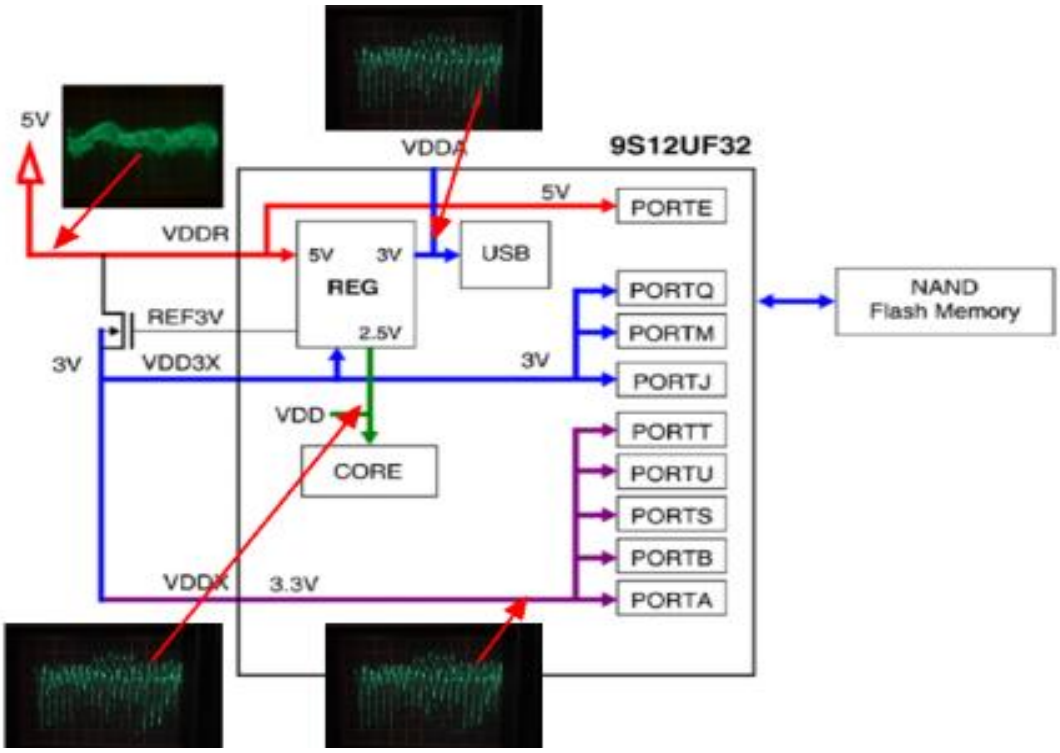


Figure 36: Freescale Flashdrive Controller Reverse Coupling

Figures 35 and 36 show examples of typical reverse noise coupling that can happen in with the FTDI USB Host Controller and the Freescale Flashdrive Controller. The FTDI USB Controller in Figure 35 contains 2 LDOs which, as we have seen in Figure 22 of this document, show large amplitude reverse coupling for high frequency noise signals generated by logic at their regulator outputs.

Figure 36 shows the 9S12UF32 Flashdrive Controller. Even though it appears to contain 2 series pass regulators, it does contain at least 1 LDO (the 2.5V core supply), which with sufficient noise energy at its LDO output, would cause significant noise coupling back to the +5V USB native supply line.

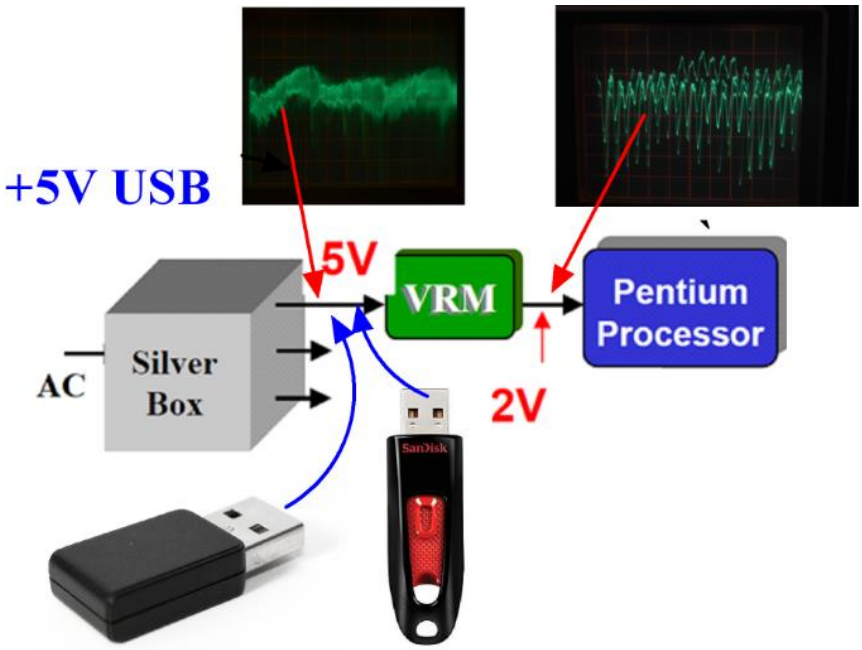


Figure 37: PowerStic and Flashdrives in Portable Devices

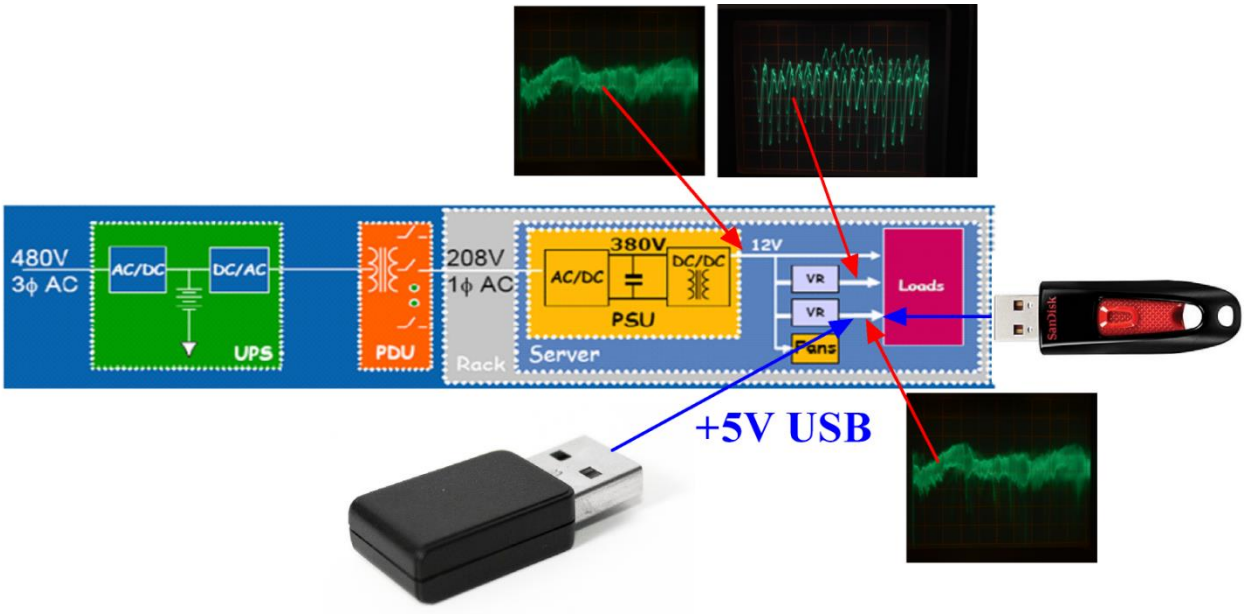


Figure 38: PowerStic and Flashdrives in Networks and Servers

Figures 37 and 38 show the USB device supply lines in portable device and large network/server based systems, the PowerStic and USB flash drives and how they share the +5V USB supply line in these systems, and the potential noise energy present on the +5V USB supply line from system reverse coupling and USB data transfer noise activity. From the Figure 37 and 38 diagrams, one can see the magnitude of this coupled noise and from where this noise is coming, and how the PowerStic device aids in noise reduction and power savings in these systems.

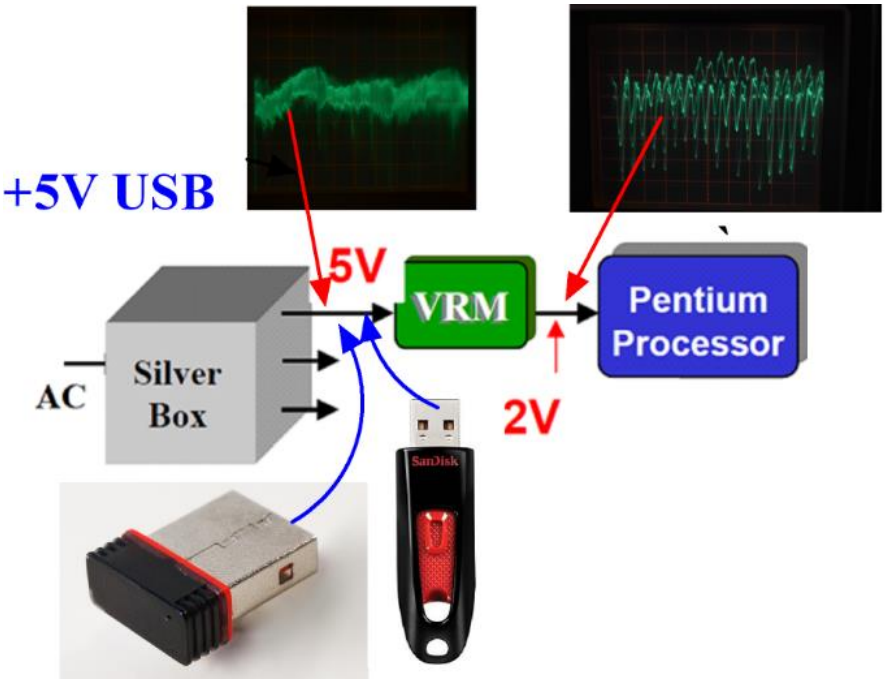


Figure 39: Exodus and Flashdrives in Portable Devices

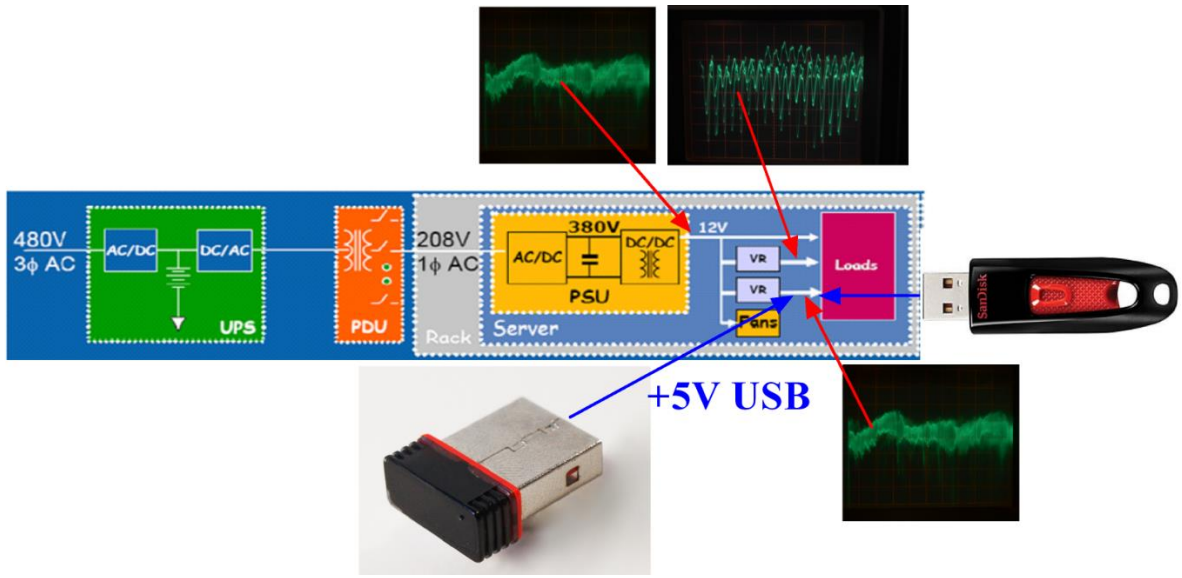


Figure 40: Exodus and Flashdrives in Networks and Servers

Figures 39 and 40 show the USB device supply lines in portable device and large network/server based systems, the Exodus and USB flash drives and how they share the +5V USB supply line in these systems, and the potential noise energy present on the +5V USB supply line from system reverse coupling and USB data transfer noise activity. From the Figure 39 and 40 diagrams, one can see the magnitude of this coupled noise and from where this noise is coming, and how the Exodus device aids in noise reduction and power savings in these systems.

Conclusion

Logic and switching circuits in systems are known to consume dynamic power. The exact mechanism of how this power is supplied, however, has not been studied or determined. High frequency reverse coupling (S21 or output to input isolation) performance in system voltage regulators is a performance metric of regulators that has not been studied or characterized by voltage regulator manufacturers. This performance metric has been considered “leakage” and unimportant in system performance until the advent of the CC-100 Power Optimizer, the PowerStic, and Exodus devices produced by CurrentRF.

This paper has shown that linear series pass and LDOs, as well as non-linear switch mode Buck regulators have varying output to input isolation characteristics

that govern how high frequency load noise and power is supplied by system regulator networks. Series pass regulators tend to block or "contain" this high frequency load noise, while LDOs and Buck regulators tend to pass the load noise to the preceding stage.

These varying regulator isolation metrics determine the high frequency supply characteristics of a given system power network, and determine where the CurrentRF CC-100 Power Optimizer, PowerStic, and Exodus devices are most effective in any given system. Series pass regulators enable local (series pass regulator output) CC-100 Power Optimizer, Powerstic, and Exodus optimized performance, while LDOs and Buck Regulators enable an optimized, somewhat remote access (+5 V USB port) for these devices. It should be also noted that a small 100nh trace inductance can increase the poor LDO and Buck regulator high frequency reverse isolation, enabling local containment of high frequency, dynamic load noise to the output of any regulator.

For more on this subject or CC-100 Power Optimizer, PowerStic, or Exodus information, please contact the following:

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http://www.CurrentRF.com.
Also, see the **MicroWave Journal** Article,
"Tapping into a New RF Energy Source found in Digital Processing Circuits.pdf" under the"**Power Optimizer**" pushbutton at **http://www.CurrentRF.com**