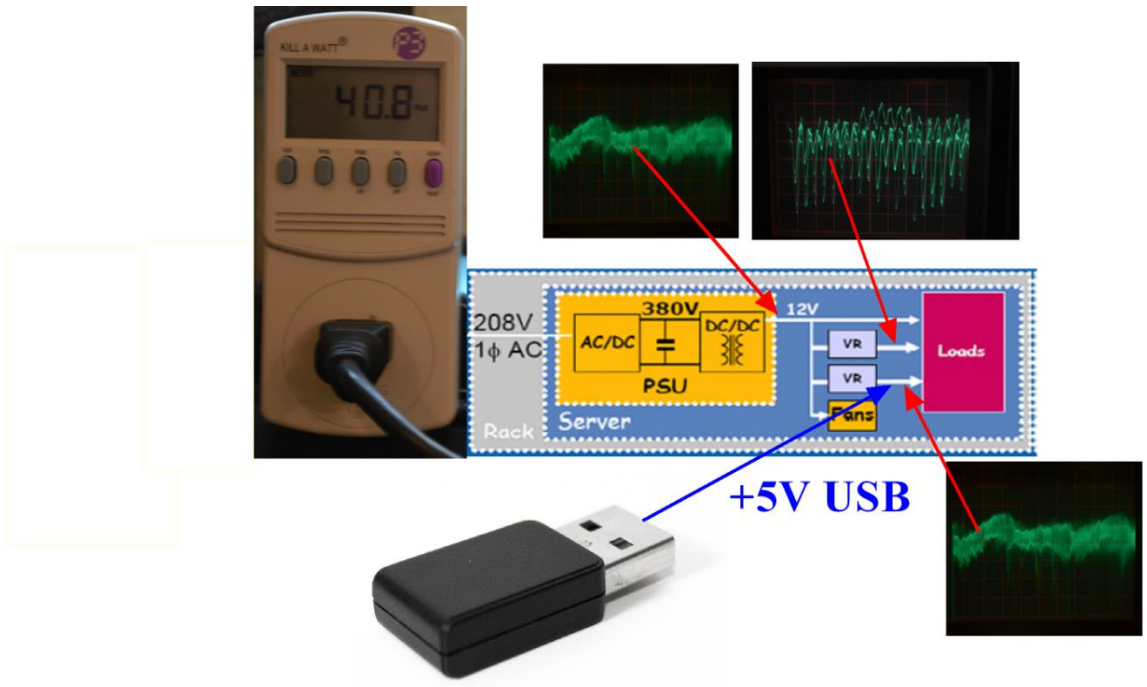
PowerStic Enabled Workstation and Server Power Reduction

Data Processing requires power. The greater the data processing volume and/or system clocking speed, the higher the power requirement. This document gives evidence of this processing/power relationship and the CurrentRF PowerStic function in reducing this data processing power over overhead.

Figure 1: PowerStic Power Reduction Application

Figure 1 shows the PowerStic Power Reduction Application as it applies to workstations and network servers. The application is simple. Identify an open or unused USB port on the workstation or server, and insert the PowerStic into the unused port. The PowerStic then, from that port, can harvest dynamic noise power, and recycle that harvested power back into the system, for overall system power reduction.



PowerStic Enhanced Workstation-Server System Model

Figure 2: How The Application Works

Figure 2 shows a general workstation or server architecture with the PowerStic inserted **(Patent Pending)** on the +5V USB supply. The mechanism of load noise coupling from the processor supply through the system LDOs and Buck Regulators in the system (contact CurrentRF for more information on this phenomenon) is also shown in Figure 2. System power is monitored by a commercially available Kill-A-Watt AC power meter, as shown in Figure 2, while the workstation is running a 20Mbyte PowerStic demo video (the PowerStic_test_demo included in this e-mail), loaded on the workstation desktop.

A HP Pavilion workstation was utilized as a test platform for the data gathered in this report. Since modern Operating Systems are autonomous relative to user programs, interrupting the processor in a mostly pseudo-random manner, the activity of the OS creates random activity reductions and spikes in gathered system power data. To

combat application variance, multiple, identical program (20 Mbyte video) runs were done and averaged to eliminate this inherent run to run variability.

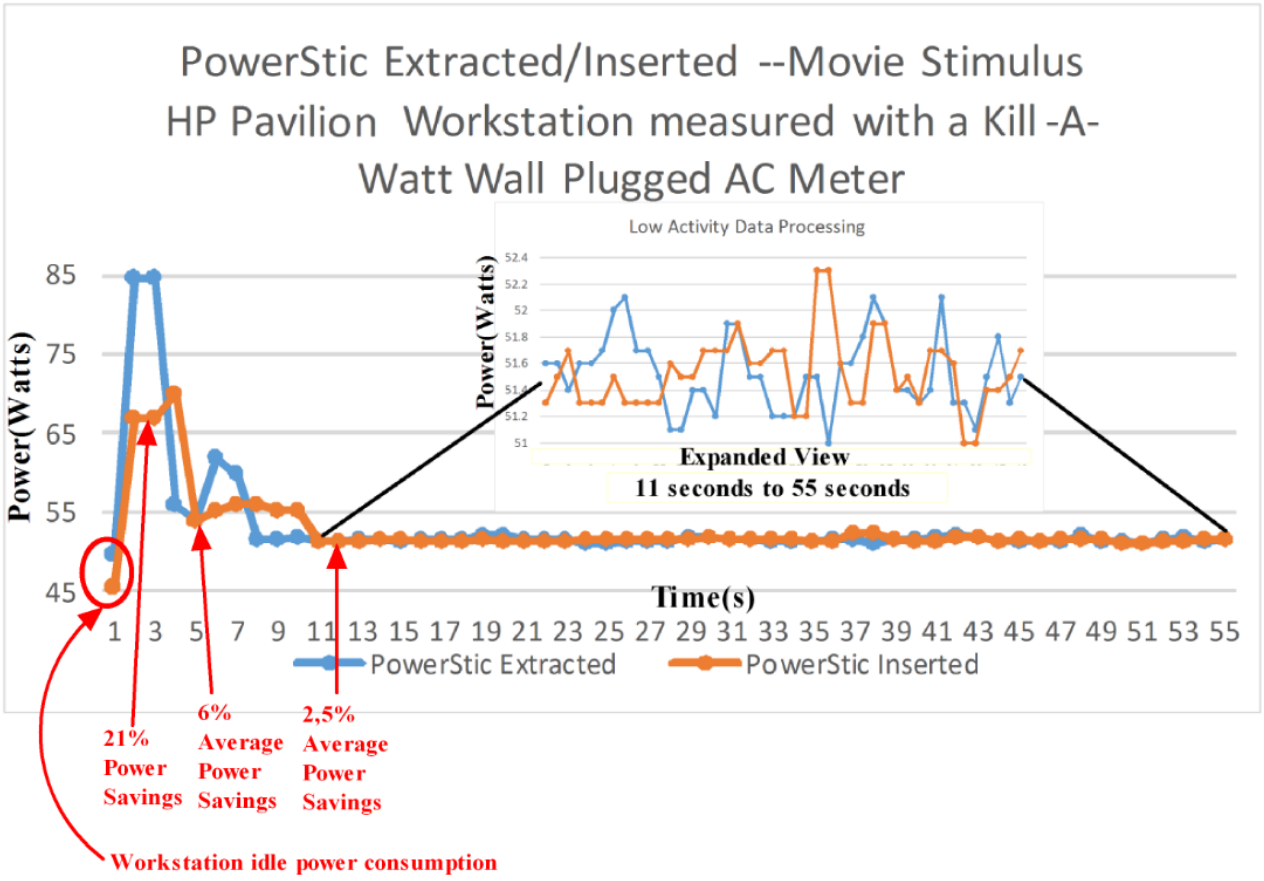


Figure 3: PowerStic Demo Video Power Profile

Figure 3 shows the power profile results generated as the result a 20 Mbyte PowerStic demo video run(the PowerStic_test_demo included in this e-mail) without(blue curve) and with(brown curve), the PowerStic inserted into the HP Pavilion workstation USB port. This data was recorded frame by frame from a video recording done of the actual PowerStic tests (see the PowerStic_example_promo video example included in this e-mail).

Just beyond the initial graph data point (second 1) in Figure 3, which shows the PowerStic extracted and inserted idle power points (50W with the PowerStic extracted, 45W with the PowerStic inserted), the Figure 3 plot shows 18W lower power, PowerStic inserted vs extracted (a 21 % total power reduction). This reduction occurs during the initial demo video loading phase from 1 to 4 seconds. Average total power reduction is then seen to range from 6% to 2.5% in the following 5 to 12 second timeframe. During the low activity data processing stage (11 to 55 seconds), one sees a 1 % to 2% total power reduction.

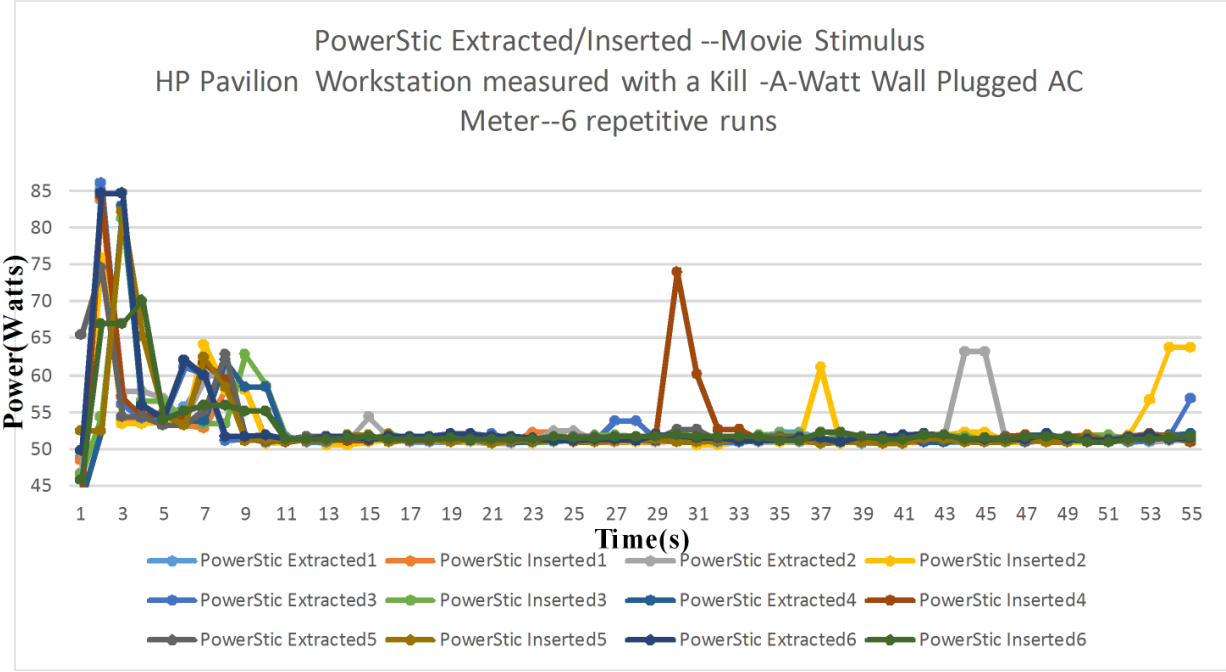


Figure 4: PowerStic Demo Video Power Profile—6 runs

Figure 4 shows the power profile results generated as the result an accumulated, 6 video, PowerStic extracted and inserted video runs (the PowerStic_test_demo included in this e-mail). This data was recorded frame by frame from a video recording done of the actual PowerStic tests.

The overall shape of the data suggests generally the same system activity as seen in Figure 3, with the exception of time offsets, activity reductions, and activity spikes due to OS interruptions. Data maximums and minimums approximately match the data found in the Figure 3 plot.

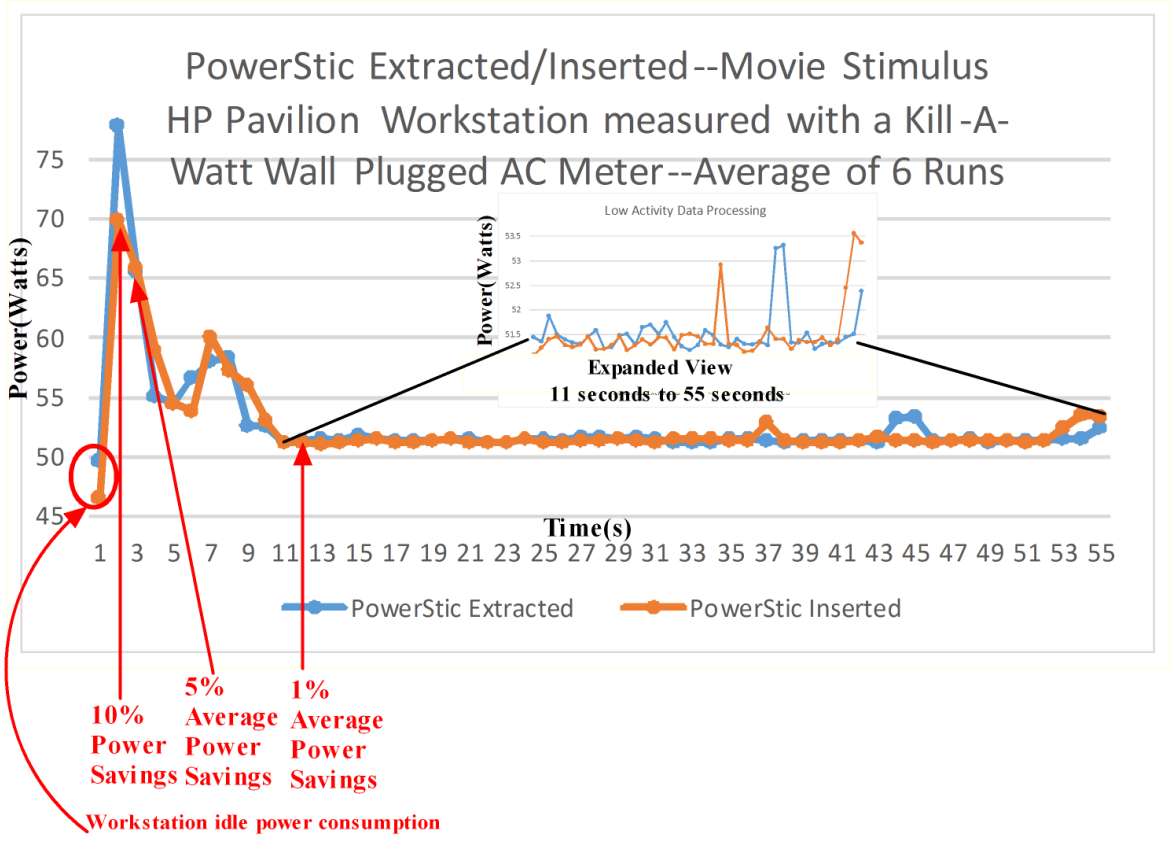


Figure 5: PowerStic Demo Video Power Profile--6 averaged runs

Figure 5 shows an averaged power profile generated as the result of an accumulated 6 runs of the 20 Mbyte PowerStic demo video run (the PowerStic_test_demo included in this e-mail) without(blue curve) and with(brown curve), the PowerStic inserted into the HP Pavilion workstation USB port. This data was recorded frame by frame from a video recording done of the actual PowerStic tests.

The overall shape of the Figure 5 data suggests generally the same system activity seen in the Figures 3 and 4 plots, minus the time offsets, activity reductions, and activity spikes present in the 6 runs of raw data shown in Figure 4. Data maximums and minimums approximately match the data found in the previous Figures 3 and 4 plots.

As with the Figure 3 and 4 plots, the Figure 5 plot, at a time just beyond the initial 1 second data points showing the PowerStic extracted and inserted idle power points (50W with the PowerStic extracted, 45W with the PowerStic inserted), the Figure 5 plot shows 8W lower power, PowerStic inserted vs extracted (a 10 % total power reduction), during the initial demo video loading phase from 1 to 4 seconds. The total power reduction then ranges on average from 5% to 1% in the 5 to 12 second timeframe. During the low activity data processing stage (11 to 55 seconds), one sees an approximate 1 % total power reduction.

Scalability

There is a substantial power difference when processing 20 Mbytes of data as compared to Gigabytes. The data taken from the 20 Mbyte PowerStic demo video used for this report suggests that the PowerStic power reduction effects on computing systems scales as the processing activity scales (e.g. observe the high activity data loading vs low processing activity areas in the Figures 3 through 6 plots and Table 1). The “heavier” data processing loads consume more dynamic power,

thus more opportunity for the PowerStic to harvest and recycle this power back into the system, creating a greater percentage of overall power reduction.

Table 1 and Figure 6 shows this relationship. The data in Table 1 is a second by second, instantaneous power analysis of the first 12 seconds of the PowerStic Extracted and Inserted, 6 run, average plot shown in Figure 5. Figure 6 shows a bar graph display of the instantaneous saved power and instantaneous percentage savings highlighted in Table 1.

As is shown in Table 1 and Figure 6, the data point at the first second in time is a measure of low, idle workstation activity. Even at this low activity level, 3 Watts are saved, producing an overall 6% power savings, the PowerStic Extracted vs Inserted in the workstation USB port.

At the 2 second marker, maximum data loading and processing is seen, producing a power spike in the PowerStic Extracted case of 77.77W. The PowerStic Inserted case at this point in time is shown to save on average 7.86W, a 10% overall reduction in operating power with respect to the PowerStic extracted case at that point in time.

At the 6 second marker, approximately 3 Watts are saved, as it was in the case of the 1 second marker, this time showing a 5% reduction in operating power.

Seconds 8, 11, and 12 show reduced power savings(2% and below), confirming that reduced data processing leads to lower power consumption, thus less opportunity for PowerStic power reduction.

Thus, as processing power increases, PowerStic power saving percentages are shown to increase.

Time(s)	PowerStic Extracted Average Power(W)	PowerStic Inserted Average Power(W)	Power Difference(W)	Power Savings Ratio	Rolling Average Power Savings Ratio
1	49.66666667	46.6	3	6%	6%
2	77.76666667	69.9	7.86	10%	8.50%
3	65.48333333	65.816666	-0.336	-0.50%	5%
4	55.13333333	58.95	-3.817	-7%	2.70%
5	54.48333333	54.4	0.083	0.10%	2.20%
6	56.65	53.816666	2.834	5%	2.60%
7	58.06666667	60.1166666	-2.05	-3.50%	1.80%
8	58.33333333	57.2	1.133	2%	1.70%
9	52.65	56.06666	-3.416	-6.40%	1.10%
10	52.58333333	53.06666	-0.483	-1%	1%
11	51.26666667	51.2	0.066	0.01%	1%
12	51.38333333	51.26666	0.47	0.02%	1%

Table 1: PowerStic Average Power Saving Scalability

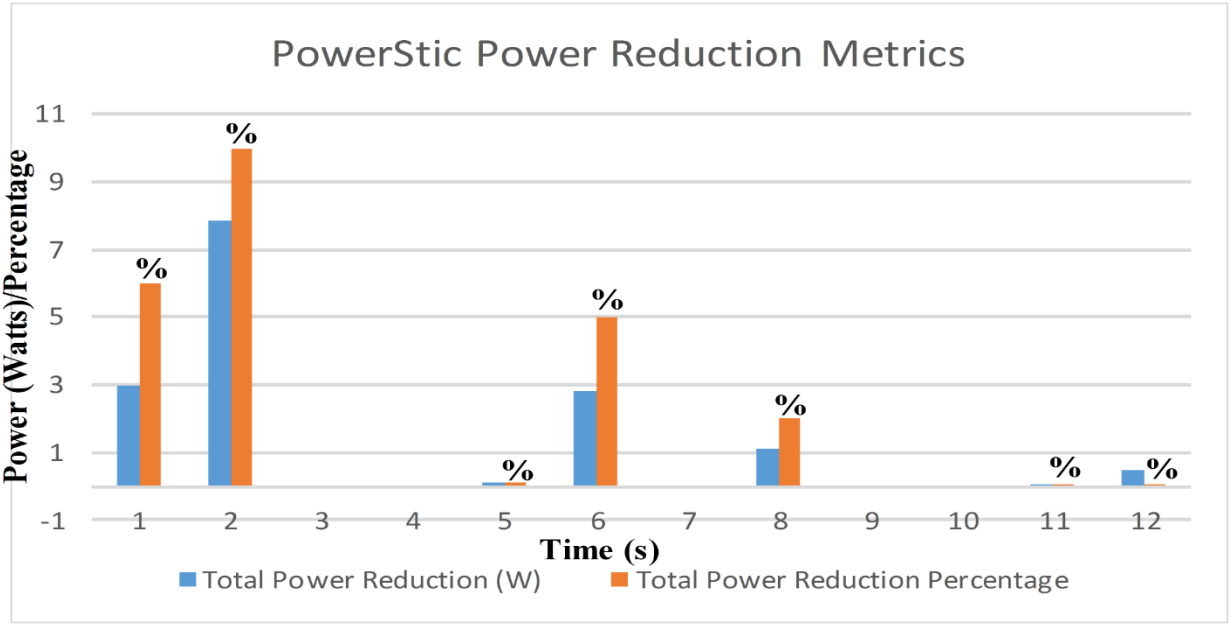


Figure 6: PowerStic Instantaneous Power Reduction Metrics

Conclusions

The PowerStic saves power in workstations, servers, and data processing systems. The Figure 5 plot shows the “smoothing results” of run to run averaging with respect to the 6 run, composite plot of Figure 4. This averaging methodology is a must, if one is to see PowerStic performance using modern operating systems. It is also seen that the numbers shown in the Figure 5 plot approximately match the numbers shown in Figures 3 and 4 plots.

The Table 1 and Figure 6 data shows that the instantaneous PowerStic power reduction scales as the consumed instantaneous, dynamic processing power scales in workstations and servers and data processing systems. With high amounts of data being processed, the PowerStic can provide substantial power and economic savings in systems where it is utilized.

For more on this subject or CC-100 Power Optimizer, PowerStic, or Exodus information, please contact the following:

543 Livingston Ct.
Discovery Bay, Ca. 94505
(209)-914-2305
Michael.Hopkins@CurrentRF.com
http://www.CurrentRF.com

For PowerStic and CC-100 characterization information, data, demo and reference designs,
contact CurrentRF at:
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Also, see the **MicroWave Journal** Article,
"Tapping into a New RF Energy Source found in Digital Processing Circuits.pdf" under the"**Power Optimizer**" pushbutton at **http://www.CurrentRF.com**