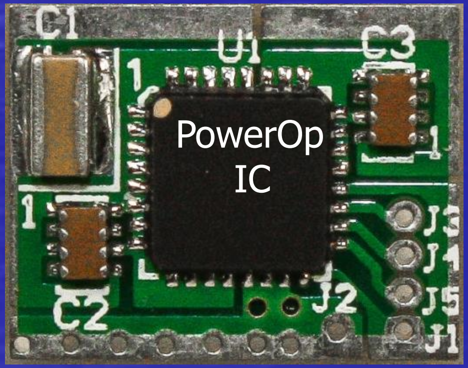
CurrentRF Power Optimizer (PowerOp)

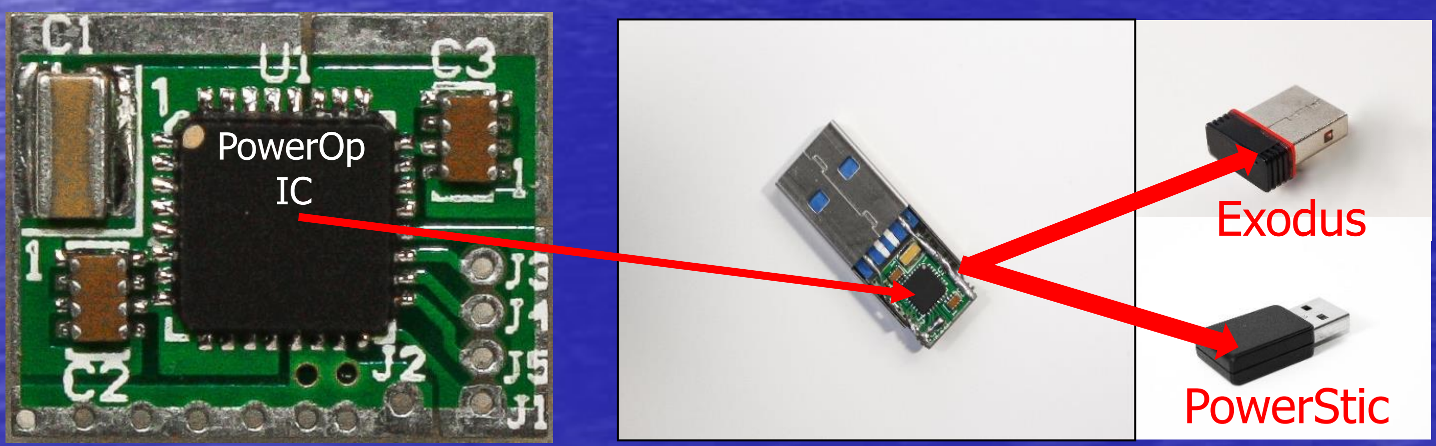
Recycle and Reuse “Throw-Away” System Circuit Noise Current with a Tiny Integrated Circuit

(5mm X 5mm X 1.2 mm)

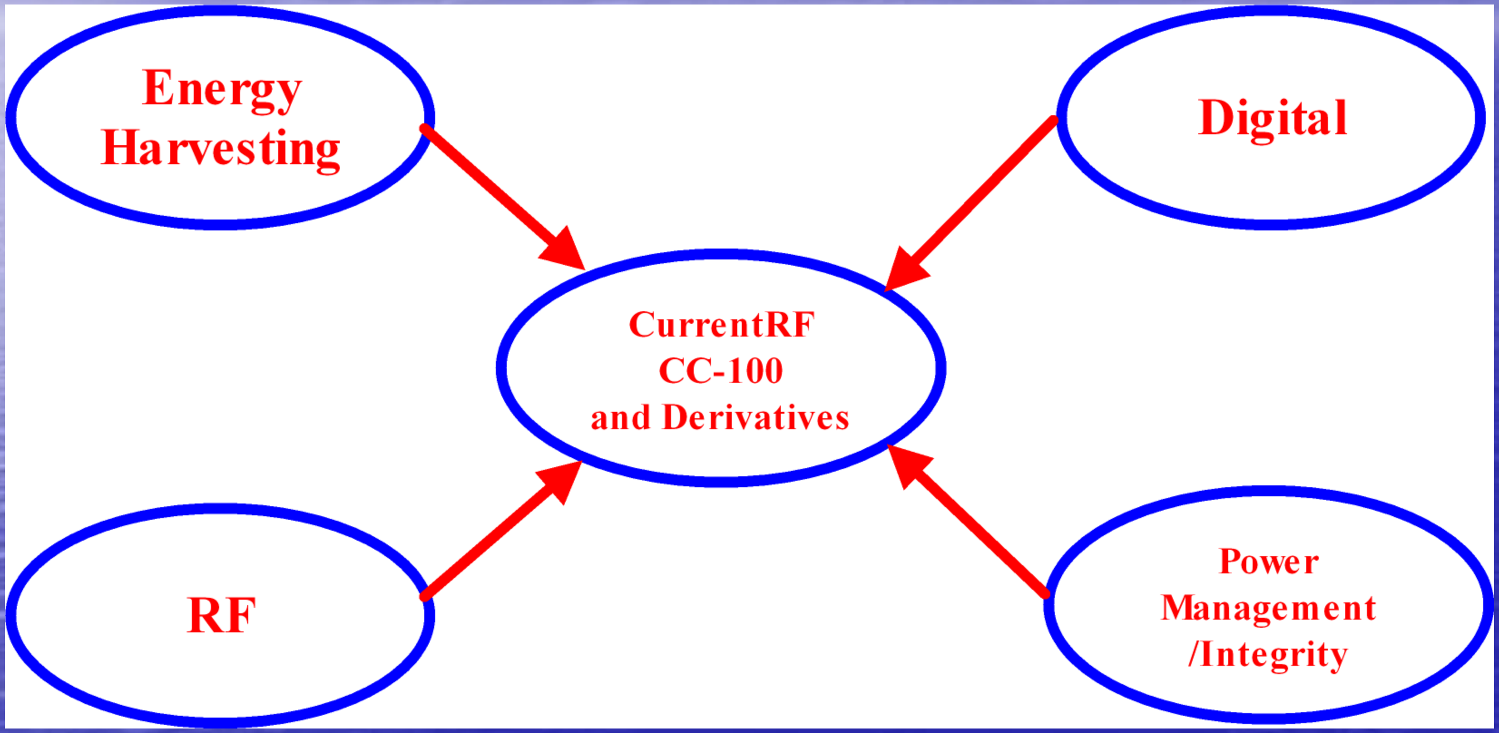


CurrentRF Power Optimizer (PowerOp) and Derivatives

Recycle and Reuse "Throw-Away" System Circuit Noise Current with a Tiny Integrated Circuit Embedded in Derivative USB Products

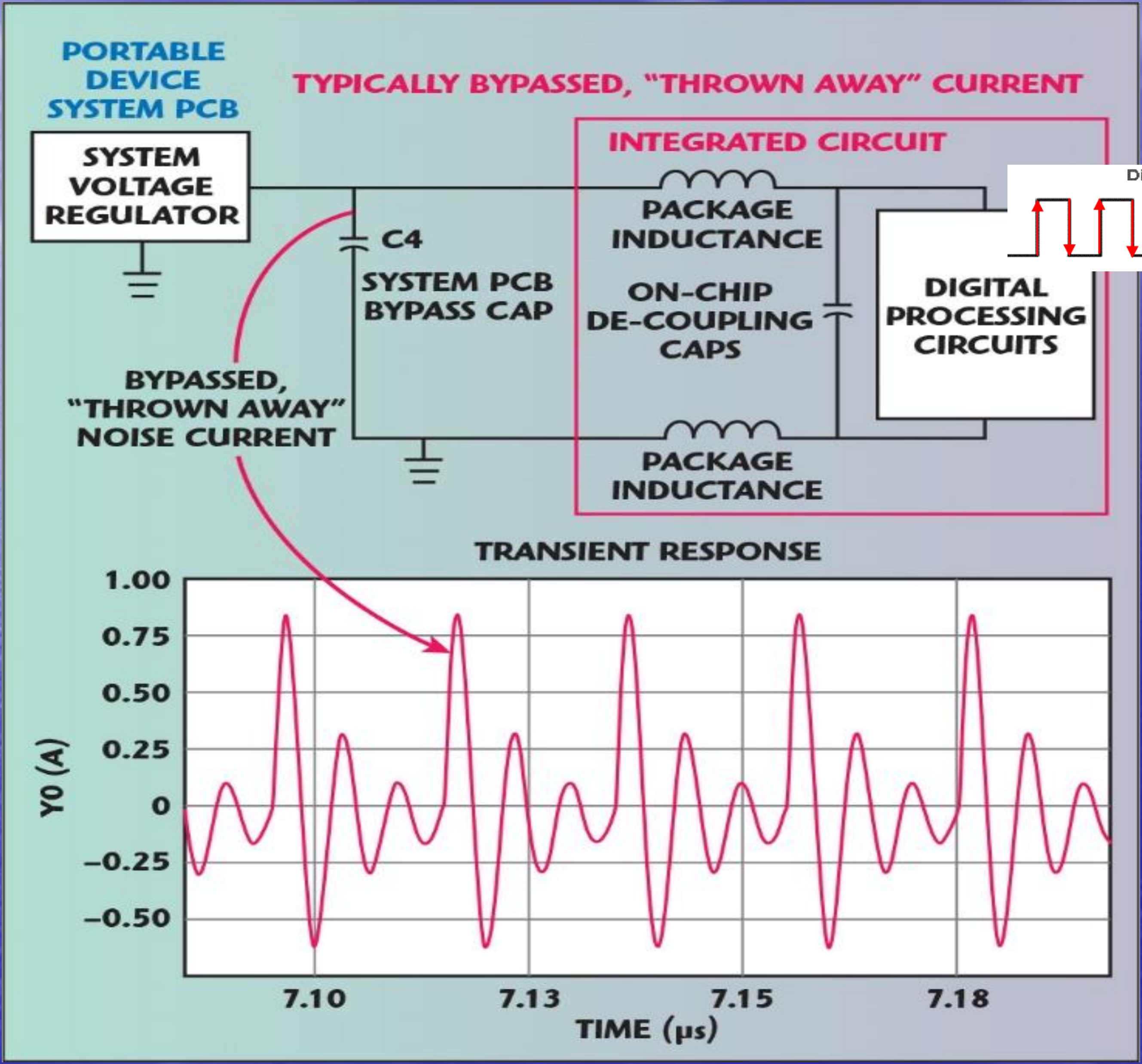


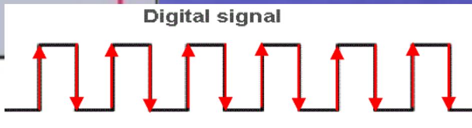
Where does this fit?



The C-100 and Derivatives bridge the 4 Engineering disciplines above

The Problem —Thrown Away, Unreachable System Noise Energy



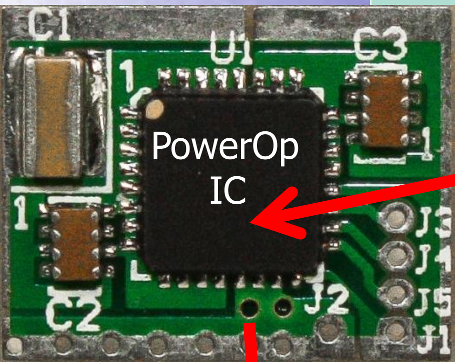


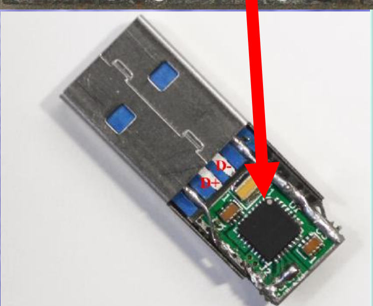
At What Level of Integration is the CC-100 Effective ?

- System/Device Level
- Printed Circuit Board Level
- Integrated Circuit Level

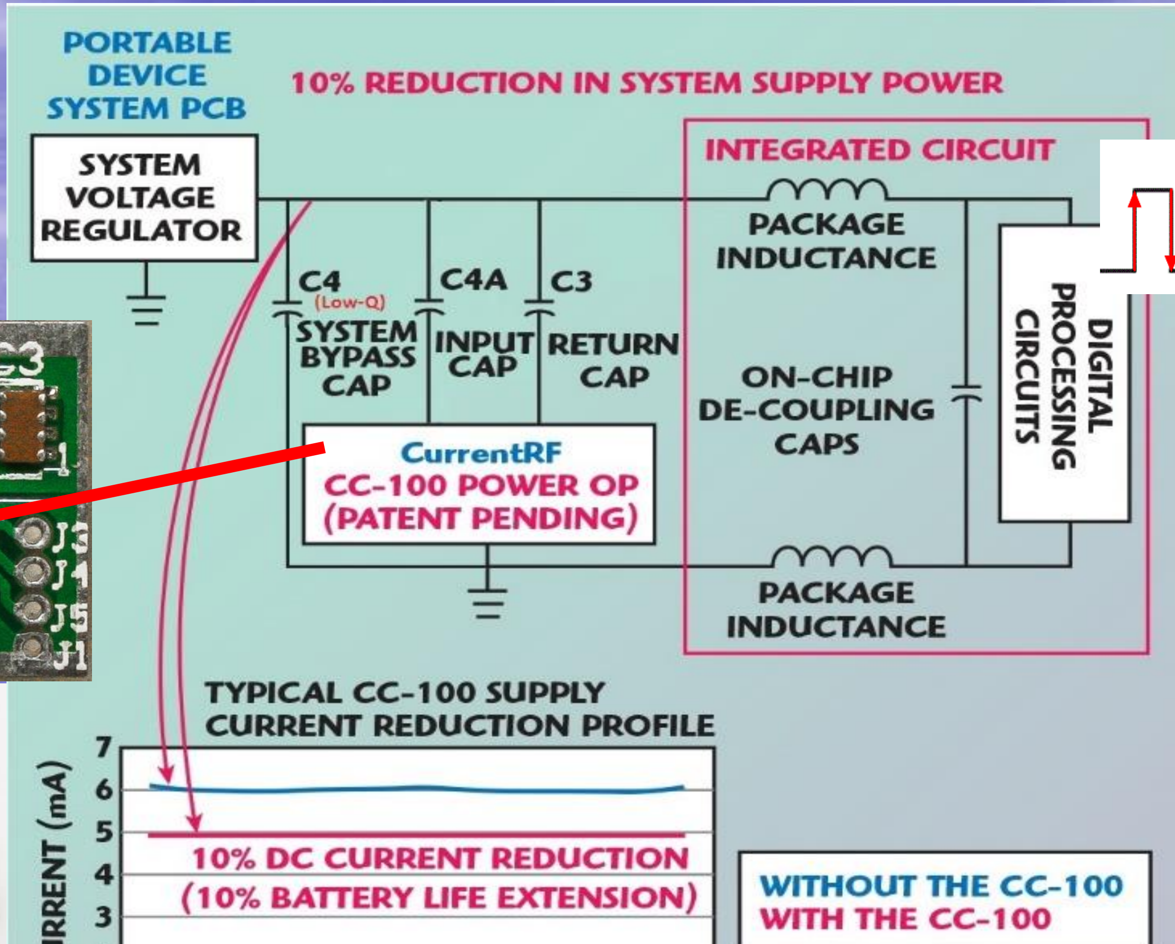
Due to the CC-100 wide bandwidth of operation,
The CC-100 device can harvest at all 3 levels of integration simultaneously,
with total system additive results

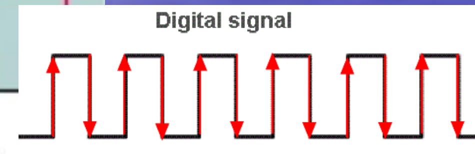
The Solution: The CC-100 Power Optimizer(PowerStic-Exodus)
Harvesting and Extracting Previously Unreachable Power at the System Level





The PowerStic (Patent Pending)



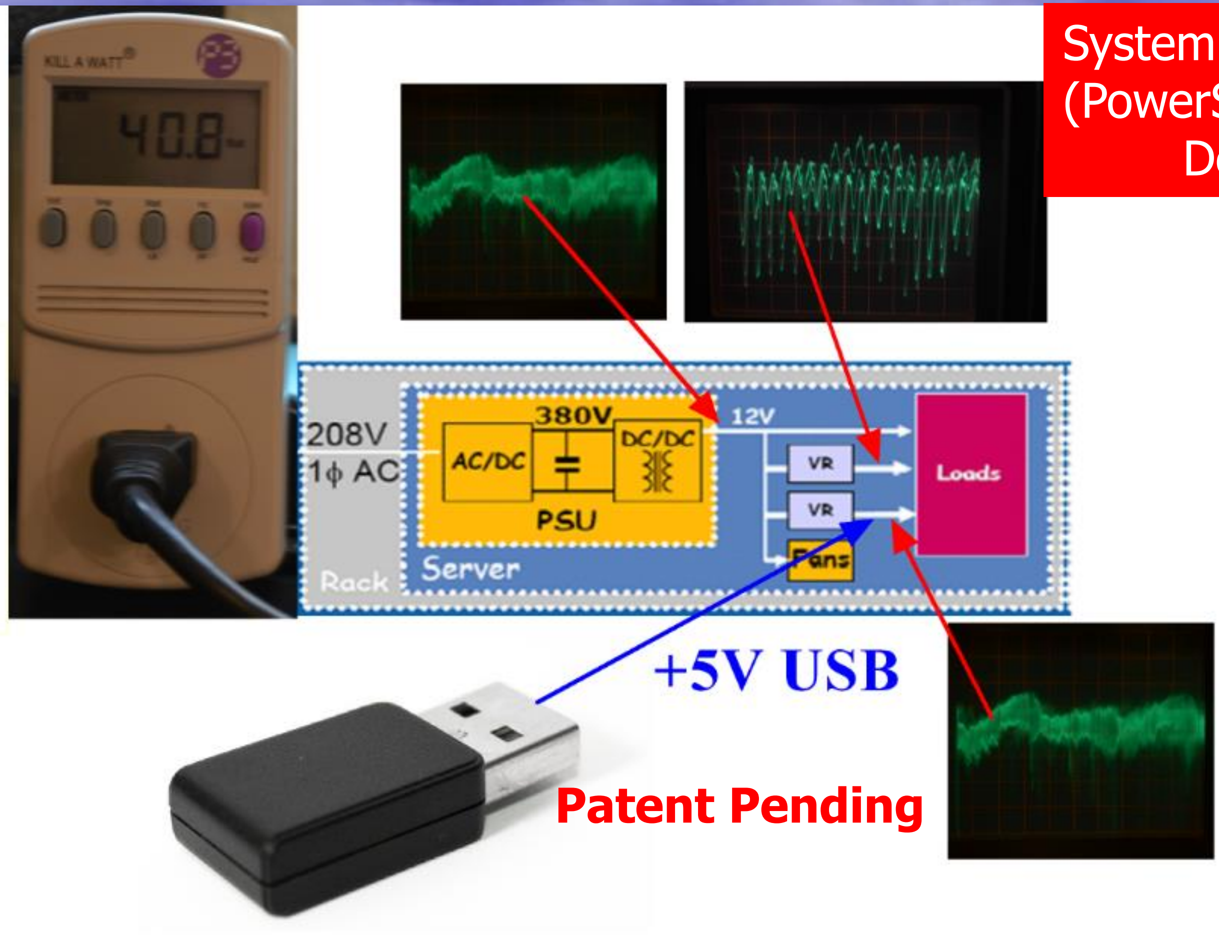


System Level Model (PowerStic/Exodus Devices)

Wall Plugged Aplications-Workstations and Servers
Harvesting and Extracting Previously Unreachable Power at the System Level

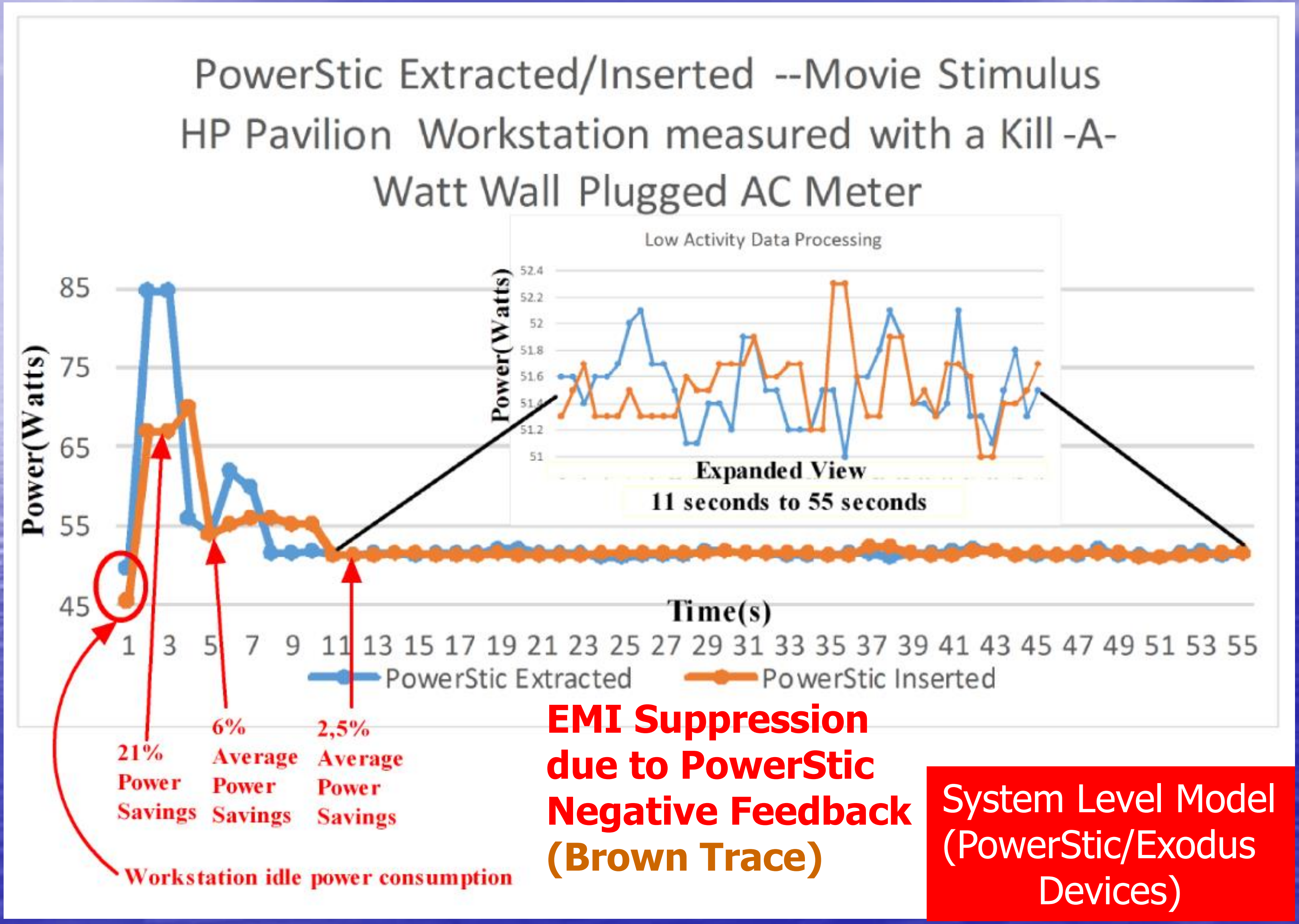
Wall Plugged Aplications-Workstations and Servers
Harvesting and Extracting Previously Unreachable Power at the System Level

System Level Model (PowerStic/Exodus Devices)



PowerStic Enhanced Workstation-Server System Model

Wall Plugged Applications-Workstations and Servers
Harvesting and Extracting Previously Unreachable Power at the System Level



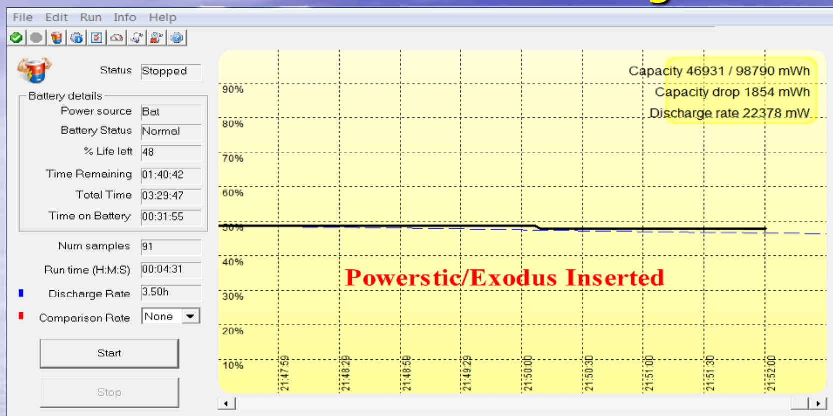
The PowerStic Extension of Battery Life

Exodus
Extension of Battery Life

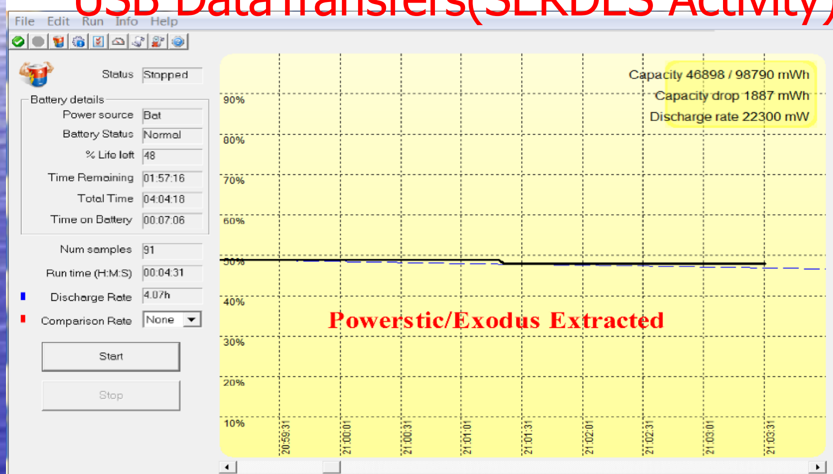
Same circuits as the PowerStic, smaller form factor

Exodus/PowerStic Laptop Average Performance

(Stimulus: "real world", variable noise, USB port, circuit activity--Measured and averaged with: BatteryMon.exe)

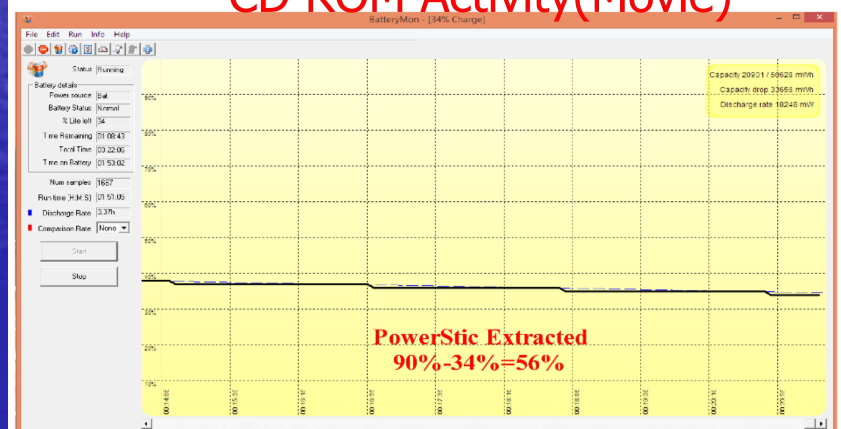


USB DataTransfers(SERDES Activity)



4 GByte flash drive to desktop data transfer (Dell Computer)
~10% Power Decrease-PowerStic Extracted vs Inserted

CD ROM Activity(Movie)

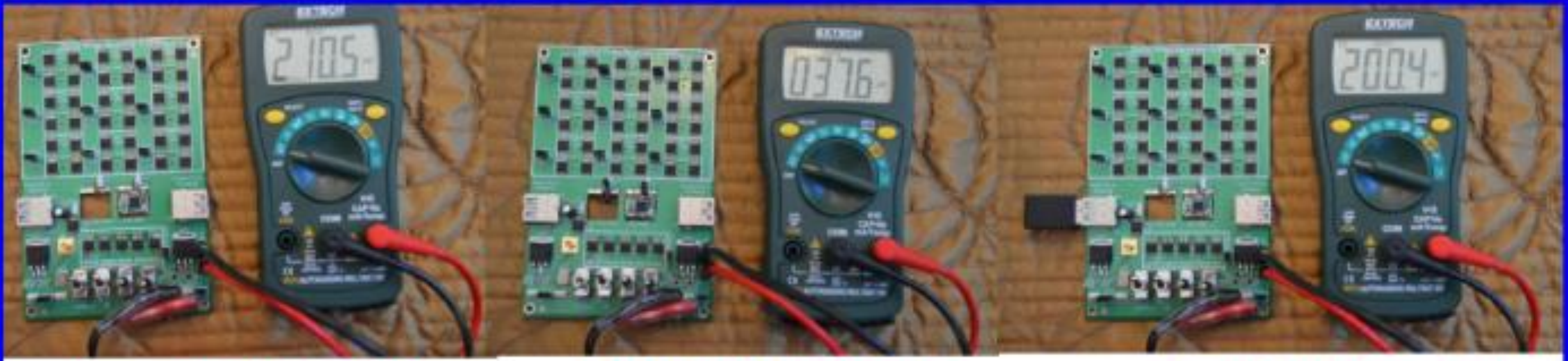


PowerStic Inserted/Extracted
Movie on Battery Performance
56%-51%/56%=~9%
9% improvement in battery life

PowerStic-Exodus Demonstration Board Performance
The PowerStic and Exodus Devices Extracted/Inserted

Number of Active LSFRs	PowerStic/Exodus Inserted (DC mA)	PowerStic/Exodus Extracted (DC mA)	Supply Current Reduction (DC mA)	Percentage Dynamic Current Reduction
9	164.7	174.1	9.4	5.4
8	147.2	154.1	6.9	4.47
7	129	134.4	5.4	4
6	111.4	116	4.6	3.9
5	93	96.7	3.7	3.8
4	74.6	77.6	3	3.8
3	56.4	58.2	1.8	3.1
2	37.7	39	1.3	3.3
1	19.1	19.8	0.7	3.5

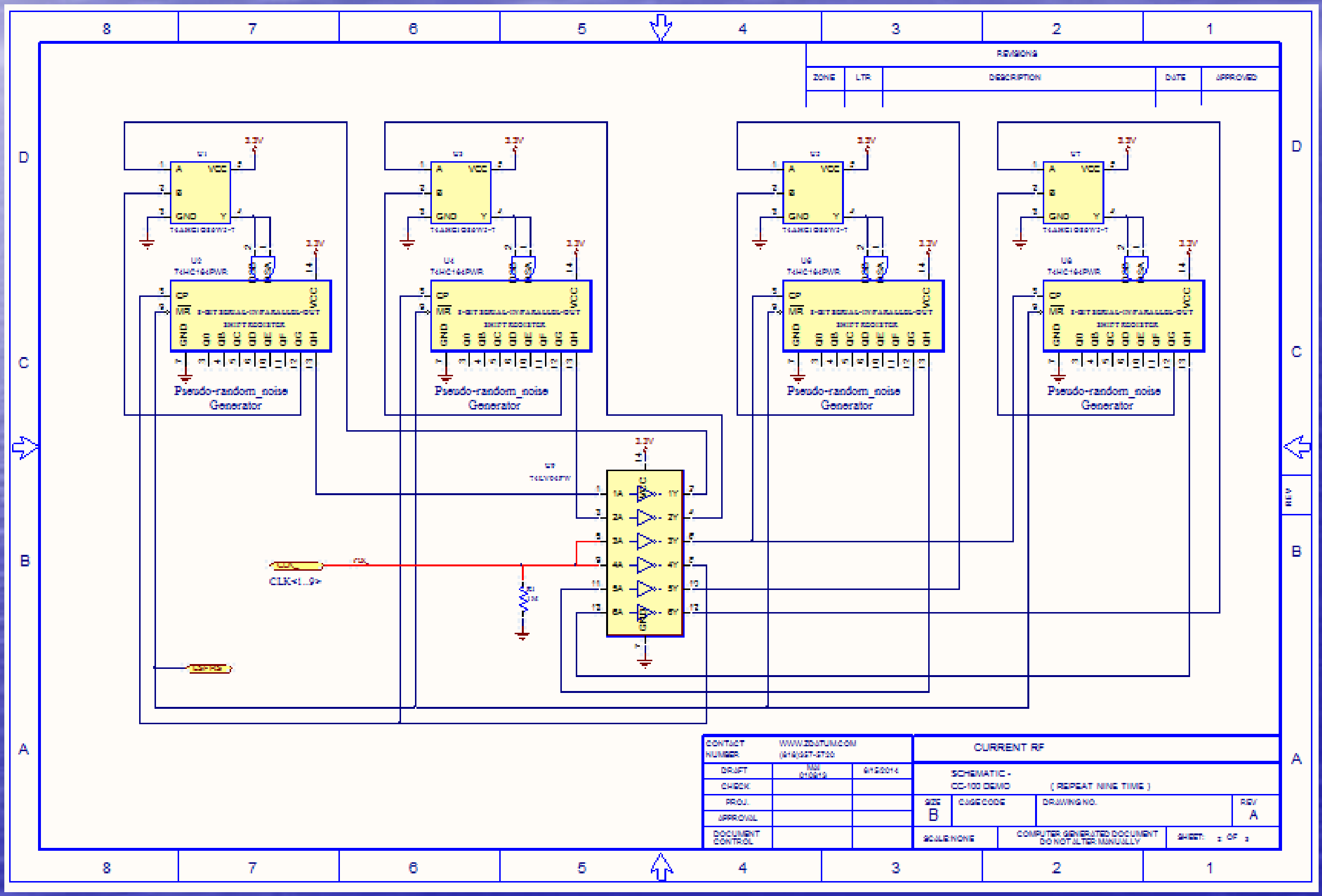
PowerStic Tests



PowerStic Extracted | LSFR DC Overhead | PowerStic Inserted

210.5mA-37.6mA=172.9mA
200.4mA-37.6mA=162.8mA
10.1mA
(10.1mA/172.9mA)X100=5.8%

Exodus-PowerStic-CC 100 Demo Board
(LSFR,Pseudo-Random Number Generator Schematic)

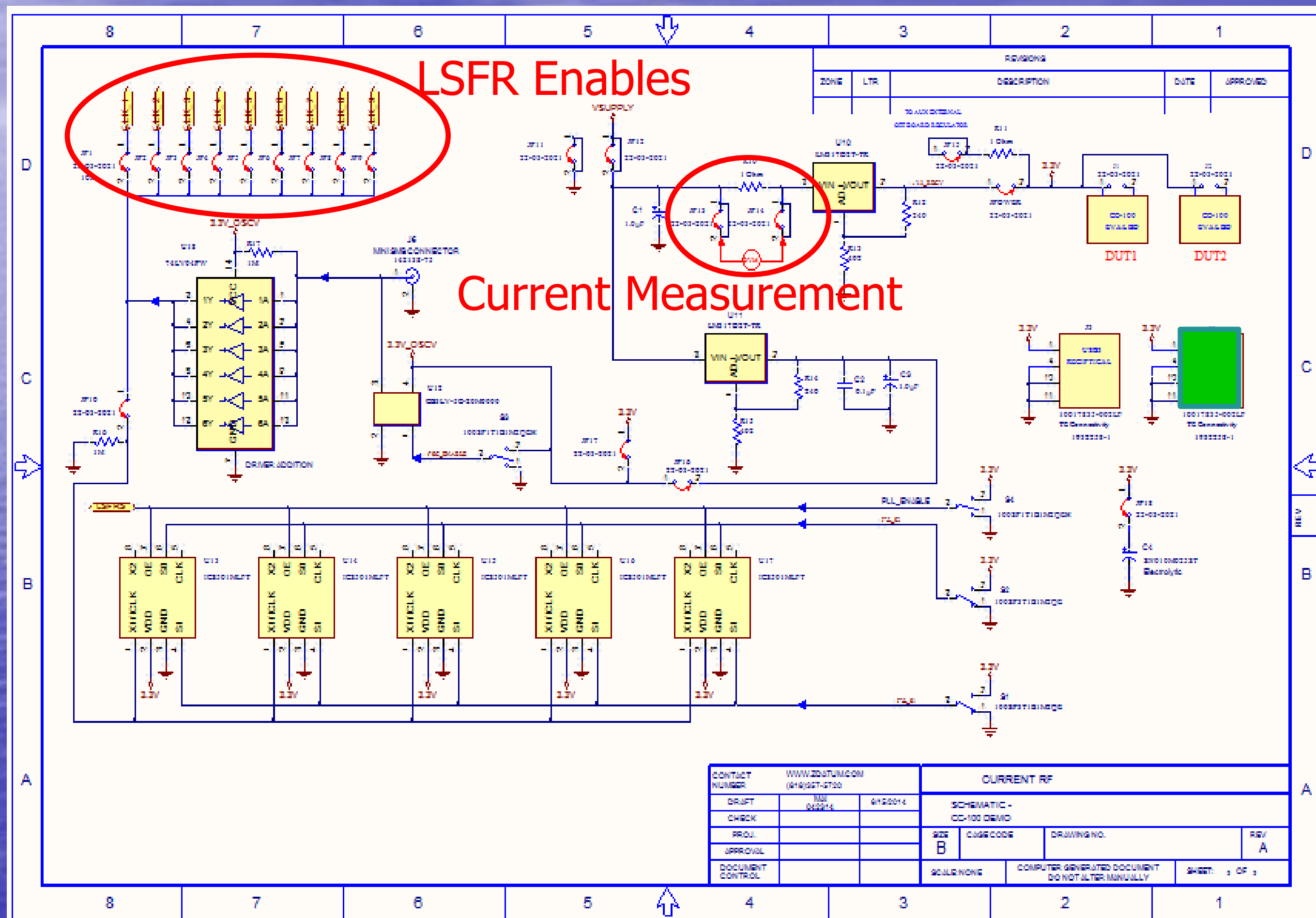


Nine groups of 4 shift registers configured as LSFR, Psuedo Random Number Generators

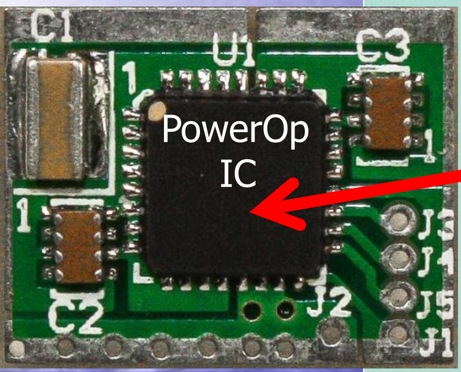
Exodus-PowerStic-CC 100 Demo Board

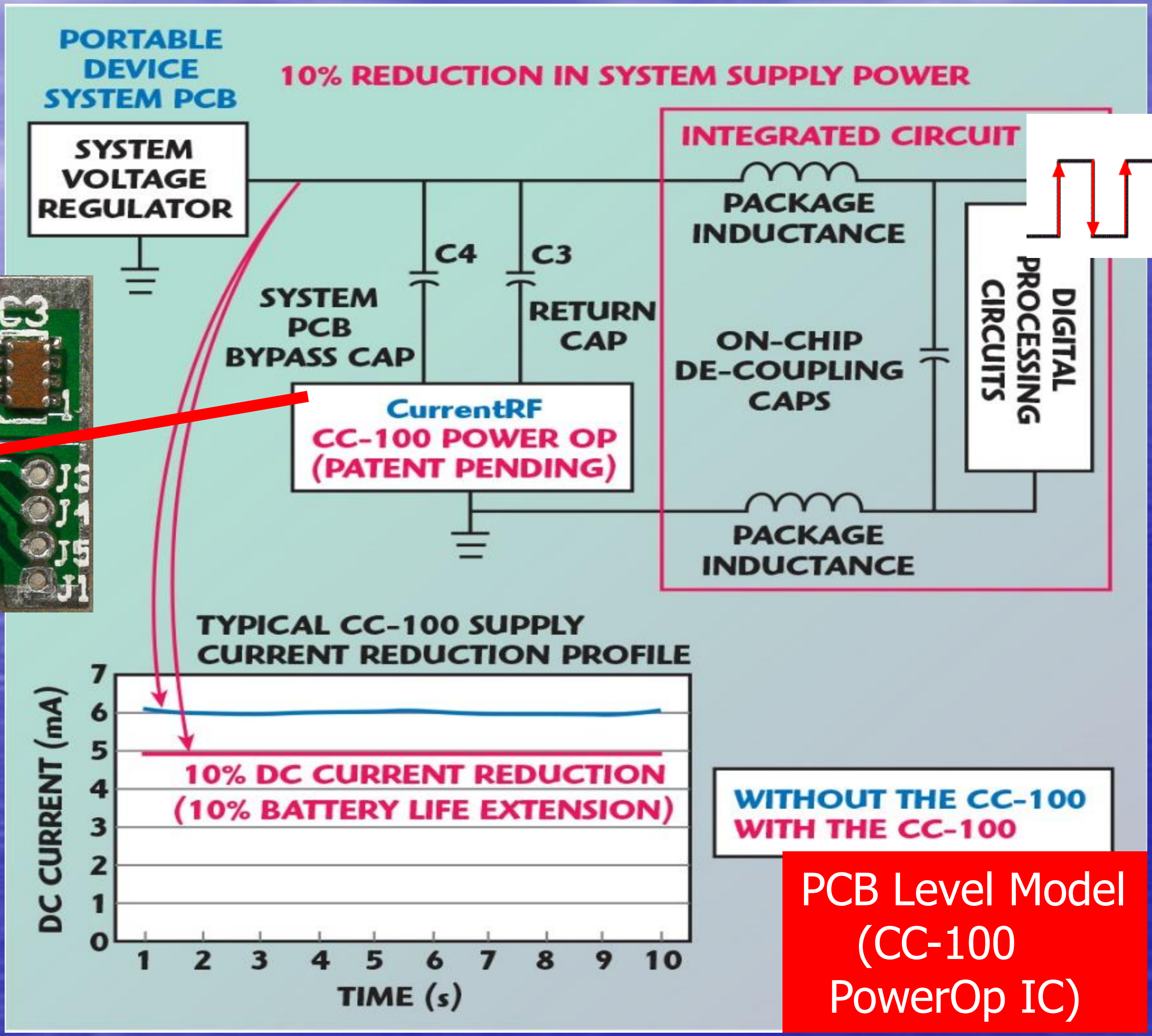
Each LSFR block consists of 4 individual Pseudo-Random Number-Noise Generators, as shown in Slide 15, that utilize a single 74HCT164 IC shift register, a single 74AHC 1G86 Exor gate, and a single 74LV07 inverter. The 9 individual LSFR blocks are enabled/disabled by individual clock input jumpers as circled in Slide 17. The 20 MHz clock is generated by a CB3LV Crystal, powered by it's own regulator (LM317) on a separated clock power plane (see Slide 17). The LSFRs are supplied by an isolated main power plane via a LM317 regulator(can be bypassed if an external regulator is desired) and supply current measurements made across a 1 Ohm resistor on the supply side of the main regulator(see the circled area in Slide 17).

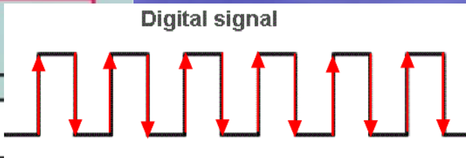
Exodus-PowerStic-CC 100 Demo Board
(Regulators/Clock Enables for LSFRs)



The Solution: The CC-100 Power Optimizer(PowerOp IC)
Harvesting and Extracting Previously Unreachable Power at the PCB Level

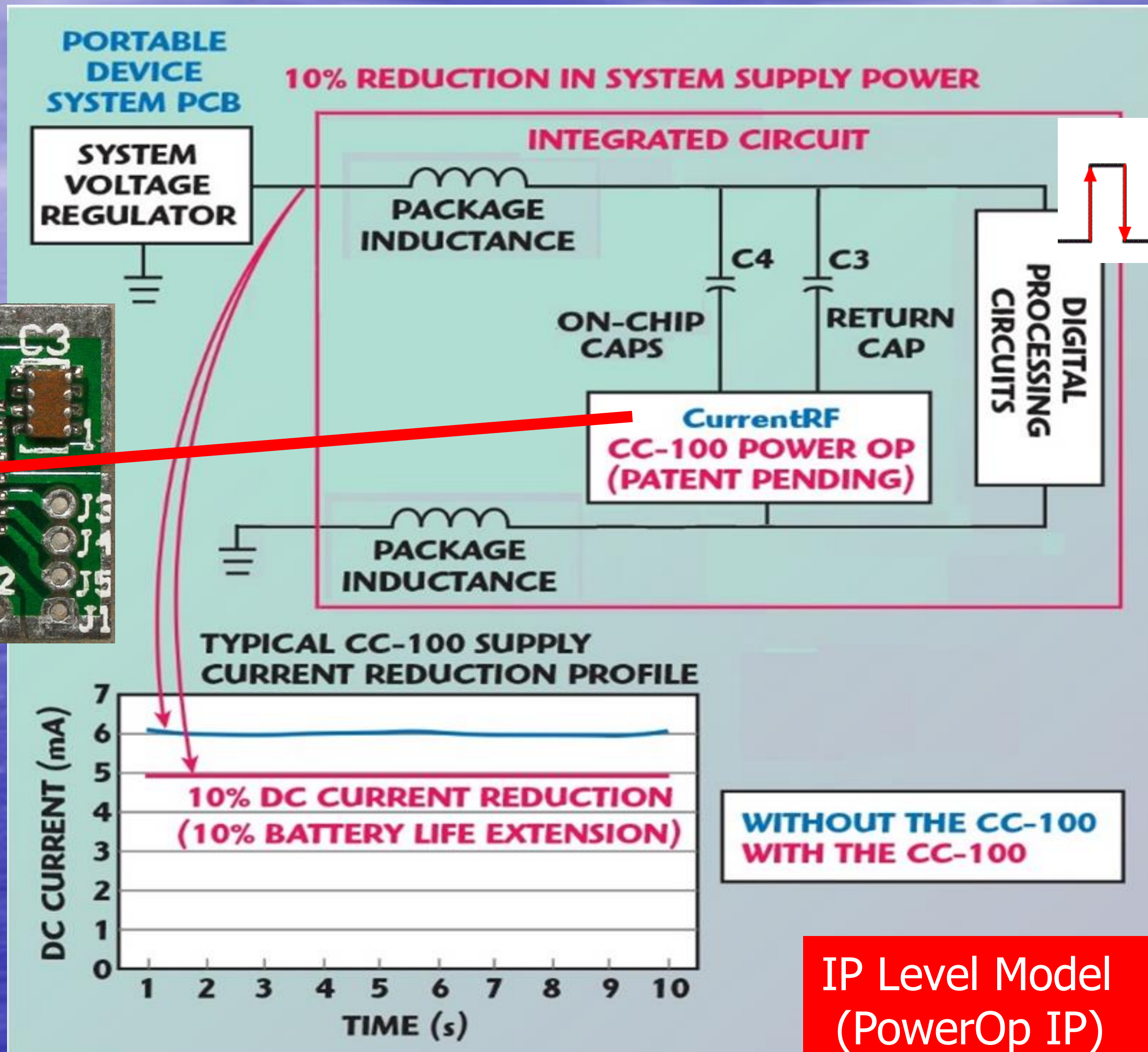


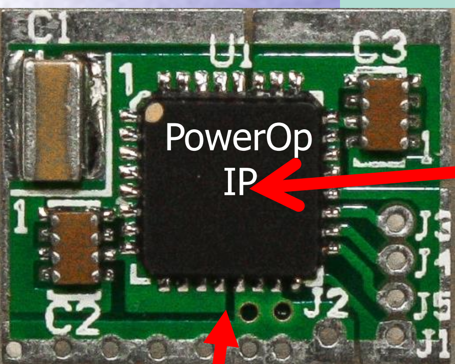


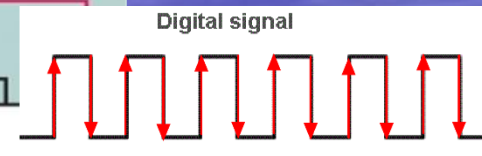


PCB Level Model (CC-100 PowerOp IC)

The Solution: The CC-100 Power Optimizer IP(PowerOp IP)
Harvesting and Extracting Previously Unreachable Power at the IC Level







The caps and the circuits scale to IP Dimensions appropriate for IC Integration

IP Level Model (PowerOp IP)

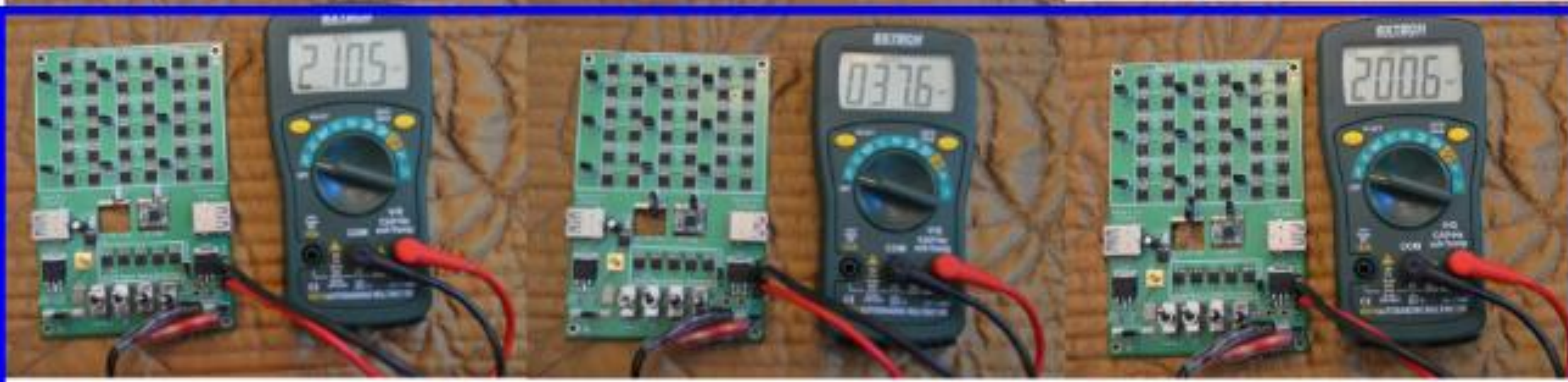
CC-100 Demonstration Board Performance
The CC-100 Extracted/Inserted

Number of Active LSFRs	The CC-100 PowerOp IC Inserted (DC mA)	The CC-100 PowerOp IC Extracted (DC mA)	Supply Current Reduction (DC mA)	Percentage Dynamic Current Reduction
9	164.7	174.1	9.4	5.4
8	147.2	154.1	6.9	4.47
7	129	134.4	5.4	4
6	111.4	116	4.6	3.9
5	93	96.7	3.7	3.8
4	74.6	77.6	3	3.8
3	56.4	58.2	1.8	3.1
2	37.7	39	1.3	3.3
1	19.1	19.8	0.7	3.5

CC-100 Average Savings→ 13uA/Mhz

As Expected, the CC-100 PowerOp IC and IP Data is almost Identical to the Exodus/PowerStic Data

CC-100 PowerOp IC and IP Tests



CC-100 Extracted | LSFR DC Overhead | CC-100 Inserted

210.5mA-37.6mA=172.9mA

200.6mA-37.6mA=163.0mA

9.9mA

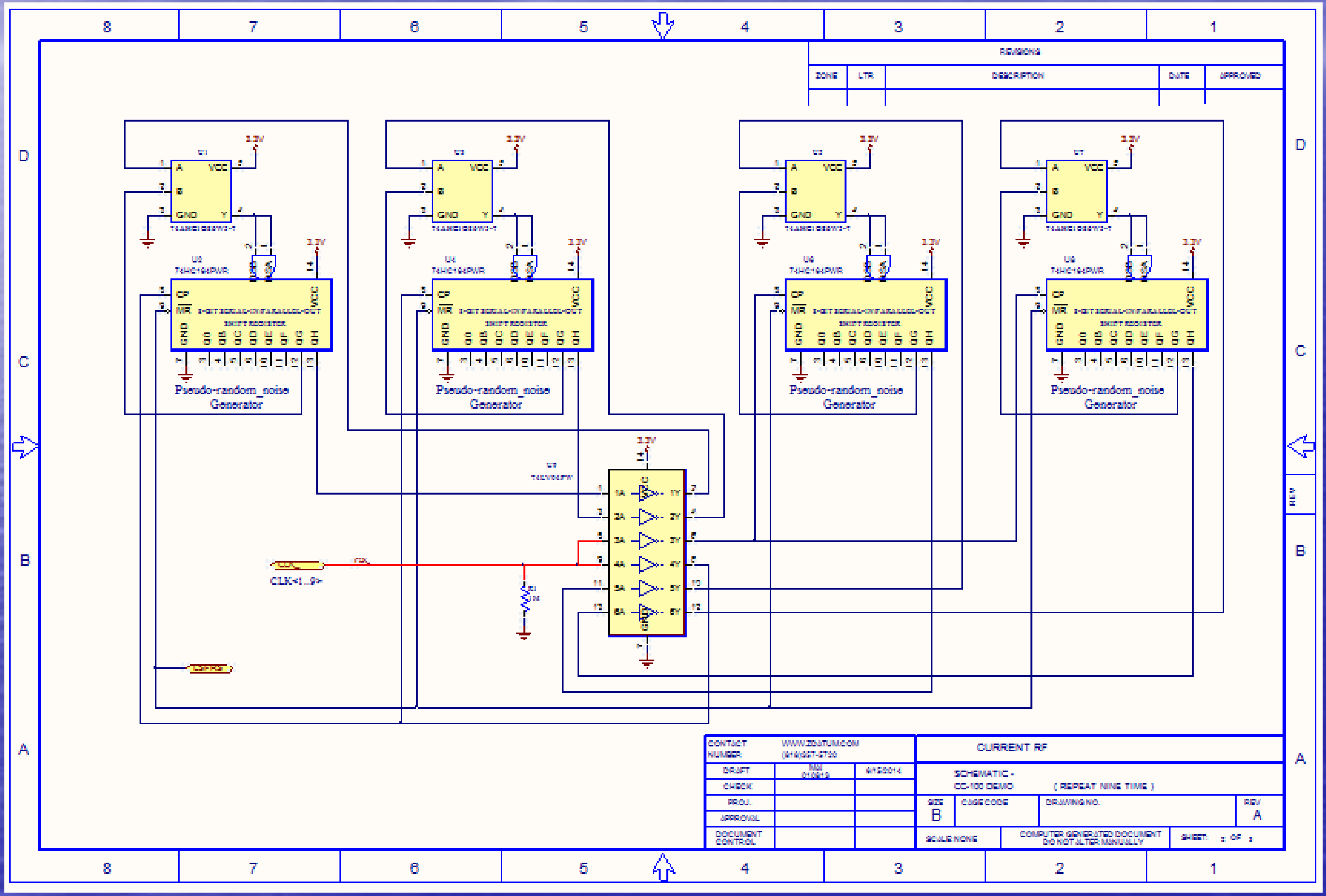
(9.9mA/172.9mA)X100=5.7%

Processor Power Savings with the CC-100 PowerOp IC and IP

Normal Processor Power | **Processor Power With CC-100 Recycling**

Source	Clock Rate(Mhz)	CC-100 Percentage Reduction	CC-100 uA/Mhz savings	uA/Mhz(processor)	uA/Mhz(with the CC-100)
CC-100 Test Board	20	5.4	13	241	228
STM8L Dynamic run with Flash	16	15.4	40	192	152
STM8L Dynamic run with Ram	16	10	26	90	64
STM8L Dynamic run with Flash	4.2	13.3	35	162	126
STM8L Dynamic run with Flash	32	15.4	40	218	178
Atmel AT32UC3A	12	15.4	40	750	710
Atmel AT32UC0512C	Unknown	15.4	40	512	472
TI MSP430F2619	Unknown	15.4	40	515	475

Exodus-PowerStic-CC 100 Demo Board (LSFR,Pseudo-Random Number Generator Schematic)

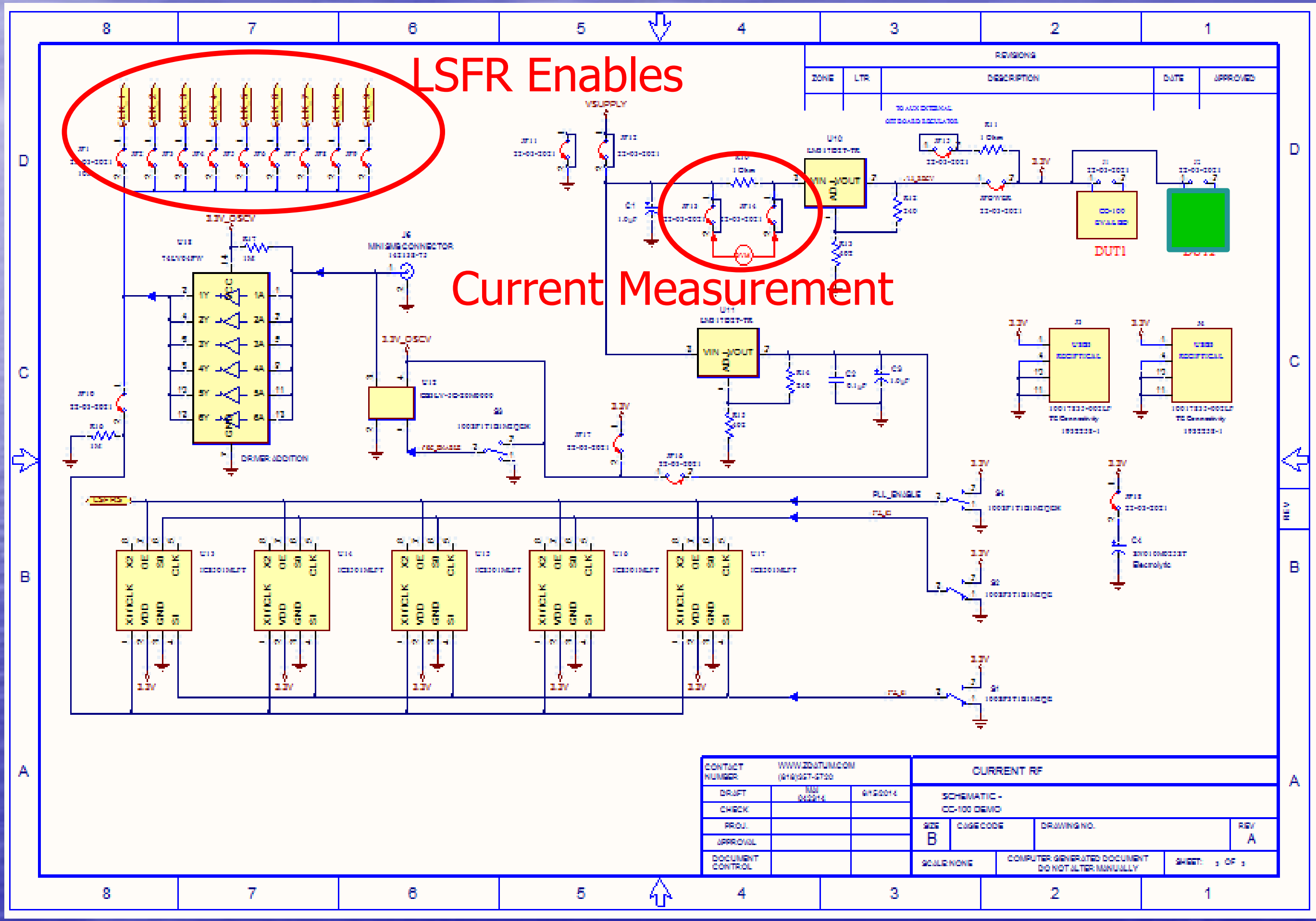


Nine groups of 4 shift registers configured as LSFR, Psuedo Random Number Generators

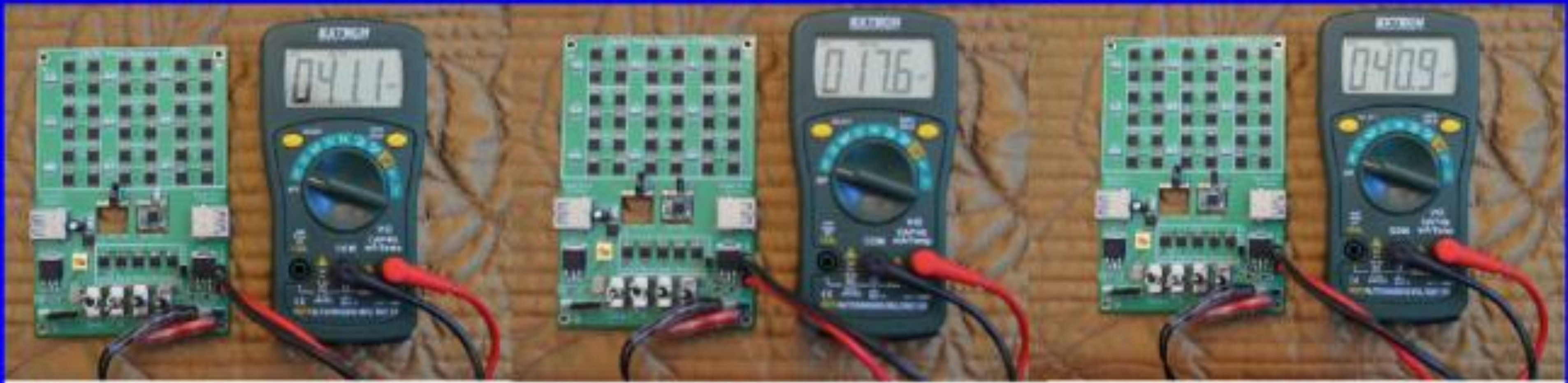
Exodus-PowerStic-CC 100 Demo Board

Each LSFR block consists of 4 individual Pseudo-Random Number-Noise Generators, as shown in Slide 23, that utilize a single 74HCT164 IC shift register, a single 74AHC 1G86 Exor gate, and a single 74LV07 inverter. The 9 individual LSFR blocks are enabled/disabled by individual clock input jumpers as circled in Slide 25. The 20 MHz clock is generated by a CB3LV Crystal, powered by it's own regulator (LM317) on a separated clock power plane (see Slide 23). The LSFRs are supplied by an isolated main power plane via a LM317 regulator(can be bypassed if an external regulator is desired) and supply current measurements made across a 1 Ohm resistor on the supply side of the main regulator(see the circled area in Slide 23).

Exodus-PowerStic-CC 100 Demo Board
(Regulators/Clock Enables for LSFRs)



CC-100 PowerOp IC and IP Tests (Minimum Sensitivity)



CC-100 Extracted | 5 PLL DC Overhead | CC-100 Inserted

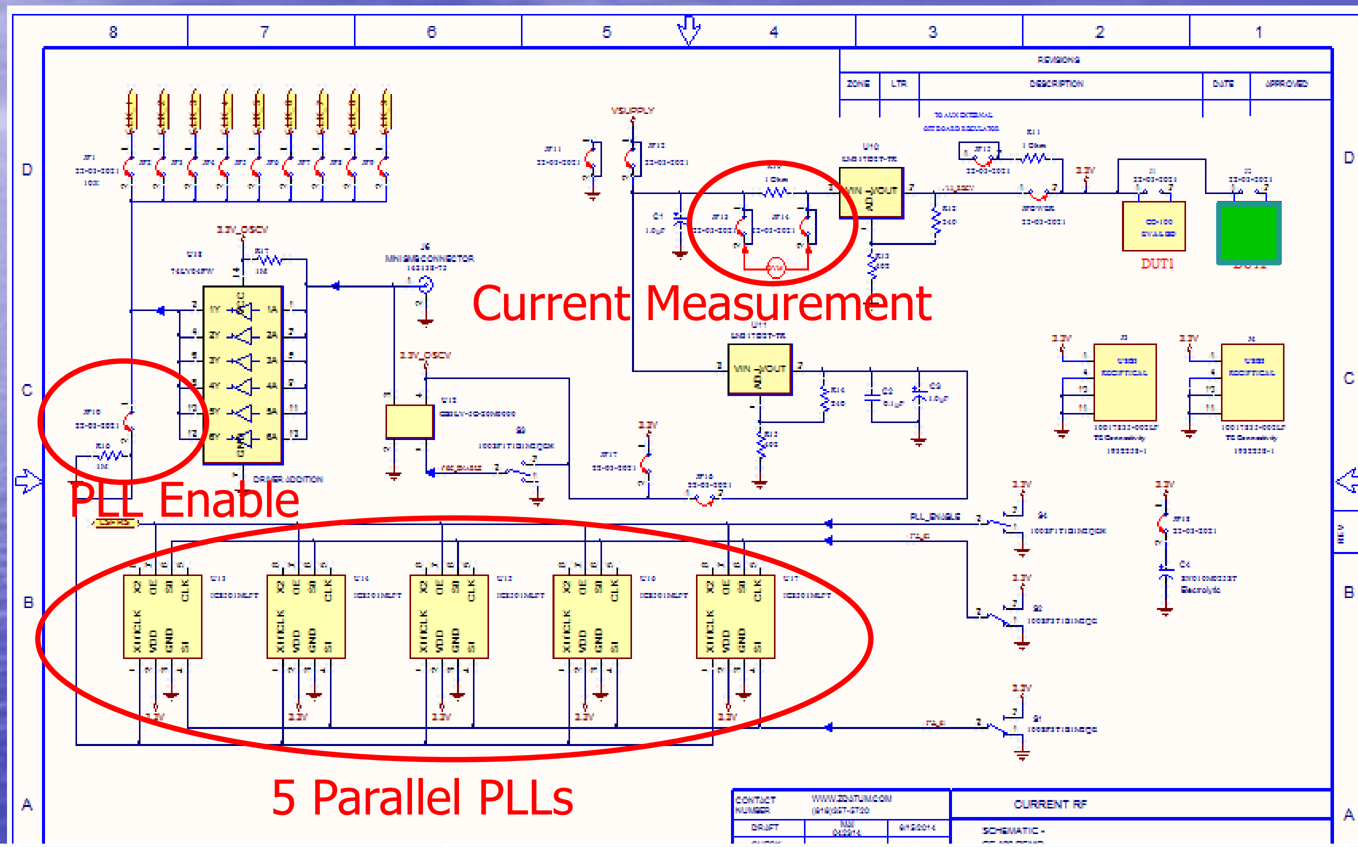
41.1mA-17.6mA=23.5mA

40.9mA-17.6mA=23.3mA

.2mA

(.2mA/23.5mA)X100=.85%

Exodus-PowerStic-CC 100 Demo Board
(Minimum Sensitivity Test)



Stimulus	CC-100 Engaged(mA)	CC-100 Disengaged(mA)	Supply Current Reduction(mA)	Percentage Reduction
Mixed Signal PLL X 5	23	23.2	0.2	1
Single PLL	4.6	4.64	0.04	1

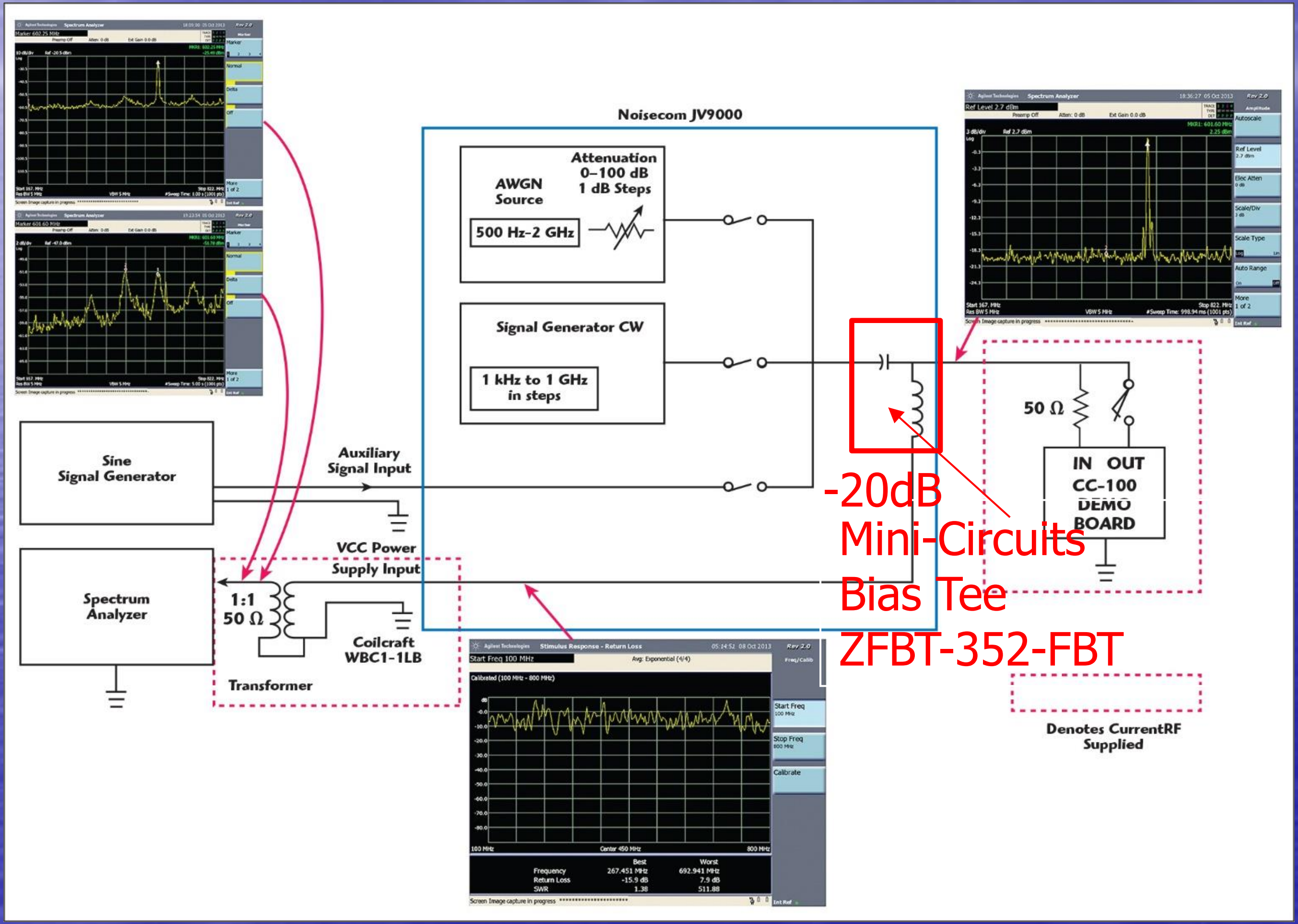
CC-100 Minimum Sensitivity→ 40uA or 2uA/Mhz

CC-100 Independent/Device Level Power Tests/Characterization

CC-100 Spectral Power Tests

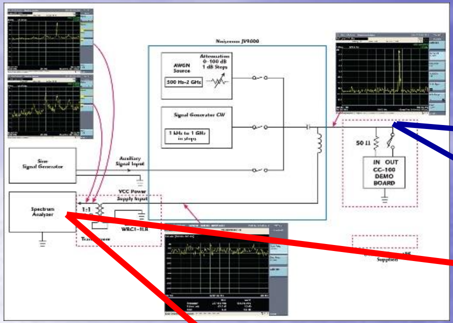
CC-100 PowerOp Spectral Power Response Test/Measurement System

(WT-Com JV9000-Agilent AT-N1996A Test/Measurement Setup)



CC-100 PowerOp Spectral Power Response Test/Measurement/Recording Procedure

(WT-Com JV9000-Agilent AT-N1996A Test/Measurement Setup)



Example Procedure (Moderate Power Data)

Raw Data from Spectrum Analyzer(dBm) (CC-100 Disengaged)

-41	-41.25	-41.5	-40.75	-41.25
-40.25	-41	-41.25	-41	-41
-41	-41.5	-41.5	-40.75	-40
-40.75	-41.5	-41.5	-41	-40
-40.75	-41	-41.25	-41	-41
-41	-41.25	-40.5	-40.75	-41.25
-41	-41.5	-41.5	-40.75	-40
-40.5	-40.75	-41.25	-41	-41
-41.5	-41	-41.5	-40.75	-40
-40.75	-41	-41.25	-41	-41

Corrected Data Through Bias Tee(dBm) (CC-100 Disengaged)

-21	-21.25	-21.5	-20.75	-21.25
-20.5	-21	-21.25	-21	-21
-21	-21.5	-21.5	-20.75	-20
-20.75	-21.5	-21.5	-21	-20
-20.75	-21	-21.25	-21	-21
-21	-21.25	-20.5	-20.75	-21.25
-21	-21.5	-21.5	-20.75	-20
-20.5	-20.75	-21.25	-21	-21
-21.5	-21	-21.5	-20.75	-20
-20.75	-21	-21.25	-21	-21

Disengaged Average(dBm)

-21.15
-20.95
-20.95
-20.95
-21
-20.95
-20.95
-20.9
-20.95
-21

+20db

Raw Data from Spectrum Analyzer(dBm) (CC-100 Engaged)

-43	-43.25	-43.5	-42.75	-43.25
-42.5	-43	-43.25	-43	-43
-43	-43.25	-42.75	-43.25	-43
-43.25	-42.5	-43	-43.25	-43.75
-42.75	-43	-43.25	-43	-43
-43	-43.25	-42.5	-42.75	-43.25
-42.5	-42.75	-43.25	-43	-43
-43	-43.5	-43.5	-42.75	-42
-43	-43.25	-43.5	-42.75	-43
-42.5	-42.75	-43.25	-43	-43

Corrected Data Through Bias Tee(dBm) (CC-100 Engaged)

-23	-23.25	-23.5	-22.75	-23.25
-22.5	-23	-23.25	-23	-23
-23	-23.25	-22.75	-23.25	-23
-23.25	-22.5	-23	-23.25	-23.75
-22.75	-23	-23.25	-23	-23
-23	-23.25	-22.5	-22.75	-23.25
-22.5	-22.75	-23.25	-23	-23
-23	-23.5	-23.5	-22.75	-22
-23	-23.25	-23.5	-22.75	-23
-22.5	-22.75	-23.25	-23	-23

Engaged Average(dBm)

-23.15
-22.95
-23.05
-23.15
-23
-22.95
-22.9
-22.95
-23.1
-22.9

+20db

Minus Bias Tee Attenuation

$$P = \left(\frac{-dBm}{10}\right) * 1mW$$

$$\frac{Vrms}{50Ohms} = Irms$$

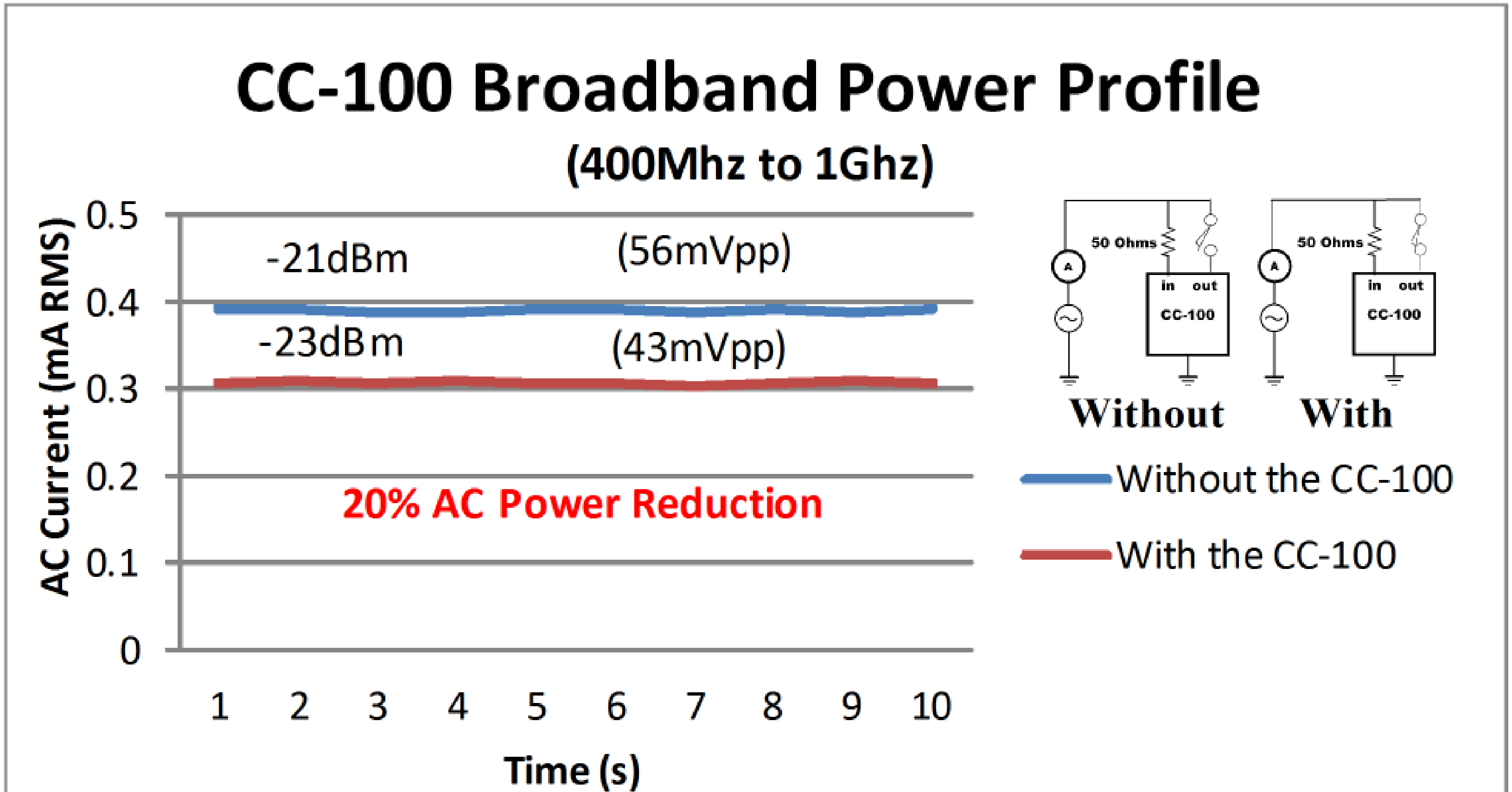
$$Vrms = \sqrt{50Ohms * P}$$

$$\frac{Vrms}{.707} * 2 = Vpp$$

CC-100 PowerOp Spectral Power Characterization Results

(JV9000/AT-N1996A Test/Measurement System)

Moderate Power

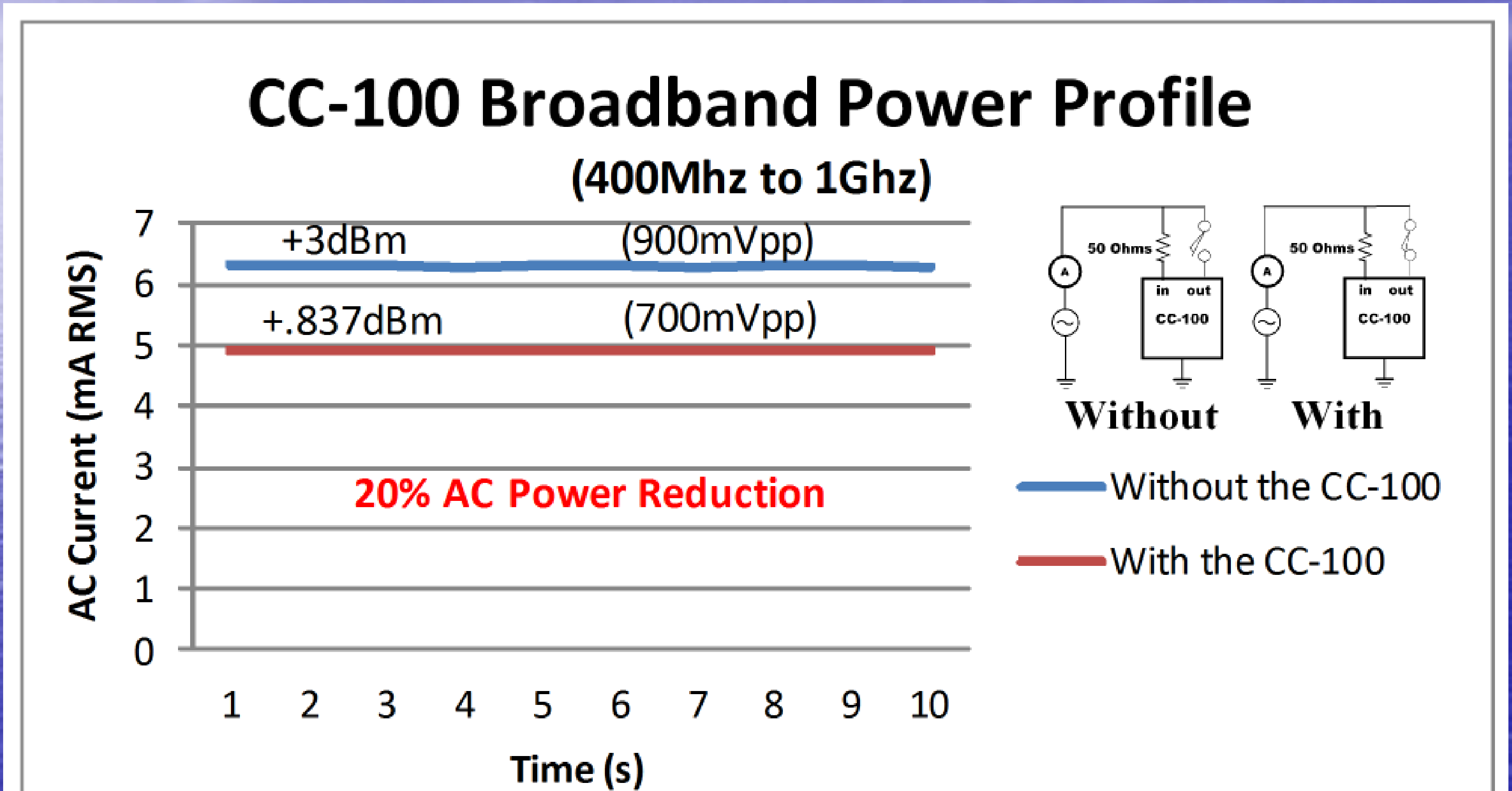


(50 Ohm resistor inserted for test purposes only)

CC-100 PowerOp Power Characterization Results

(JV9000/AT-N1996A Test/Measurement System)

High Power

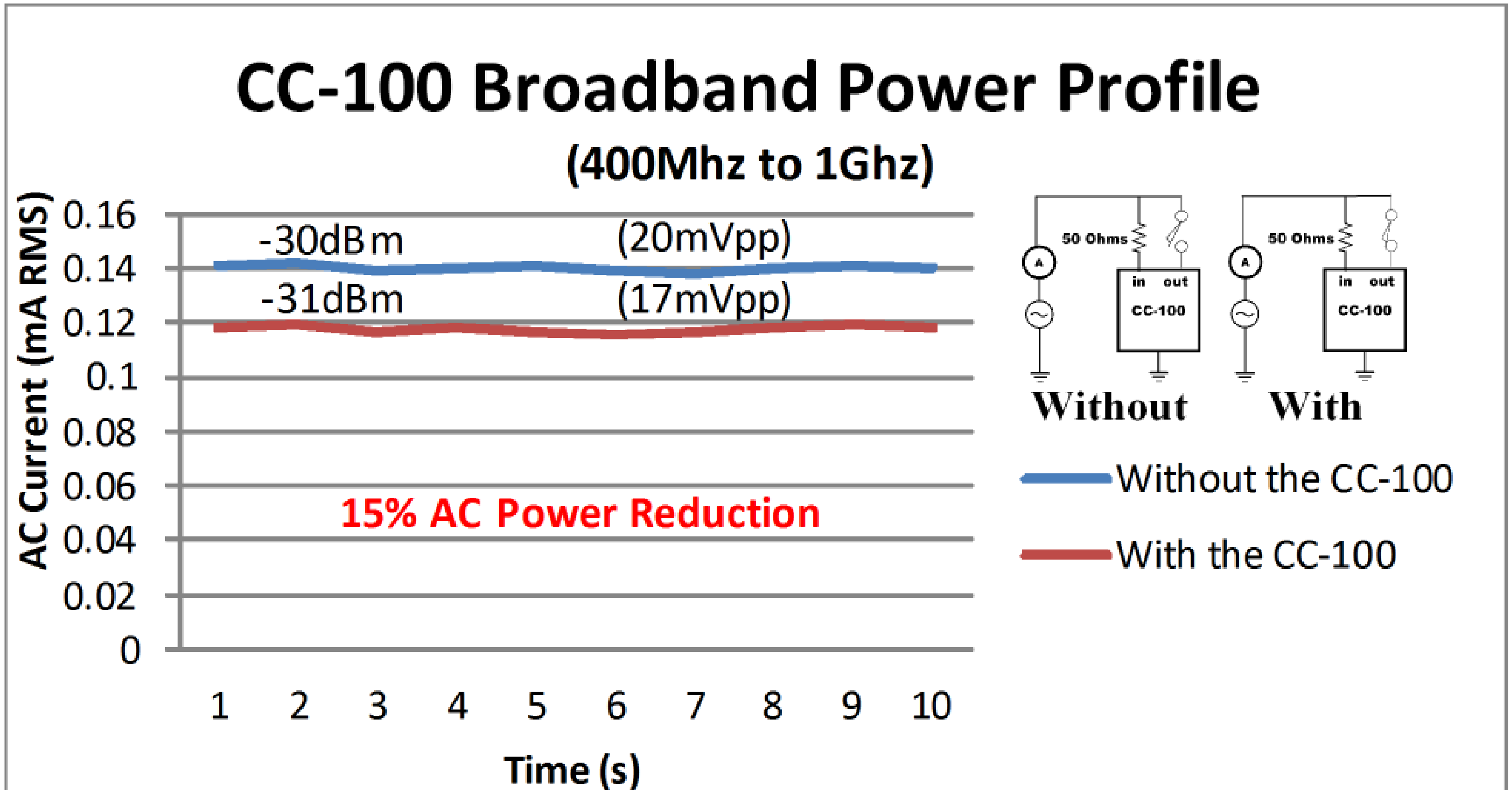


(50 Ohm resistor inserted for test purposes only)

CC-100 PowerOp Power Characterization Results

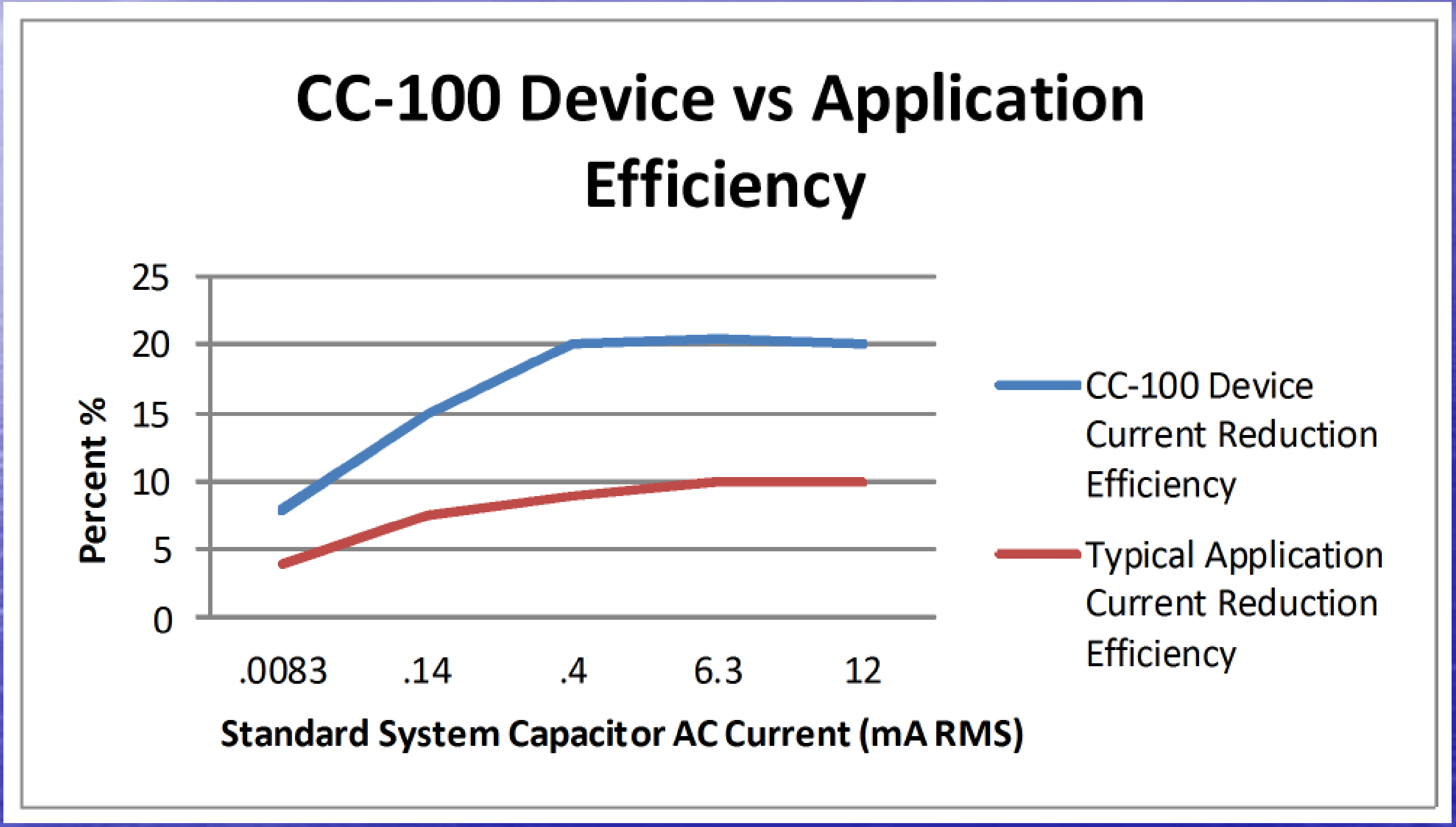
(JV9000/AT-N1996A Test/Measurement System)

Low Power



(50 Ohm resistor inserted for test purposes only)

CC-100 PowerOp Device vs Application Characterization Results



CC-100 Input Impedance/Bandwidth Tests/Characterization

CC-100 PowerOp Device Input Impedance/Spectral Response

(Agilent AT-N1996A Network/Spectrum Analyzer)

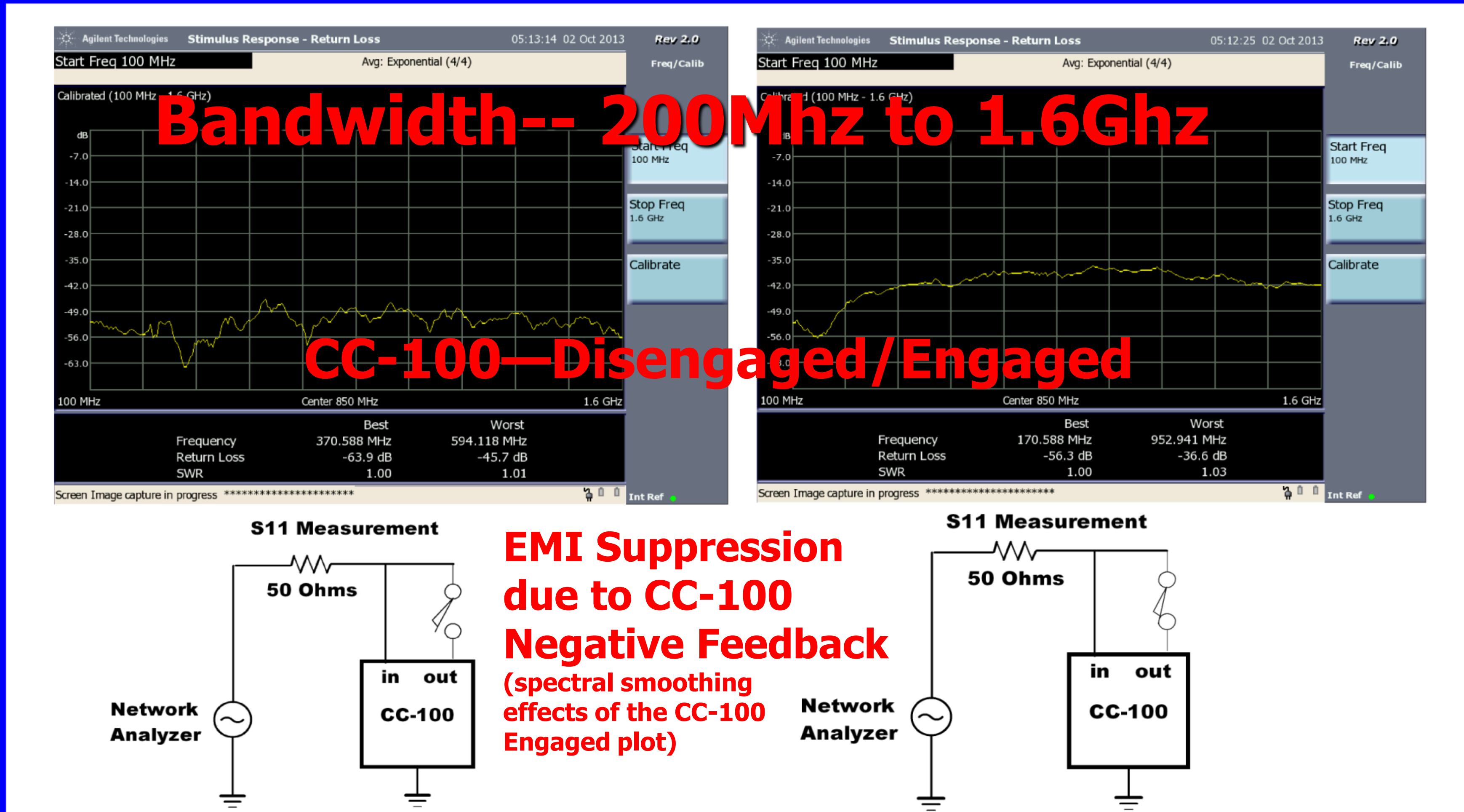
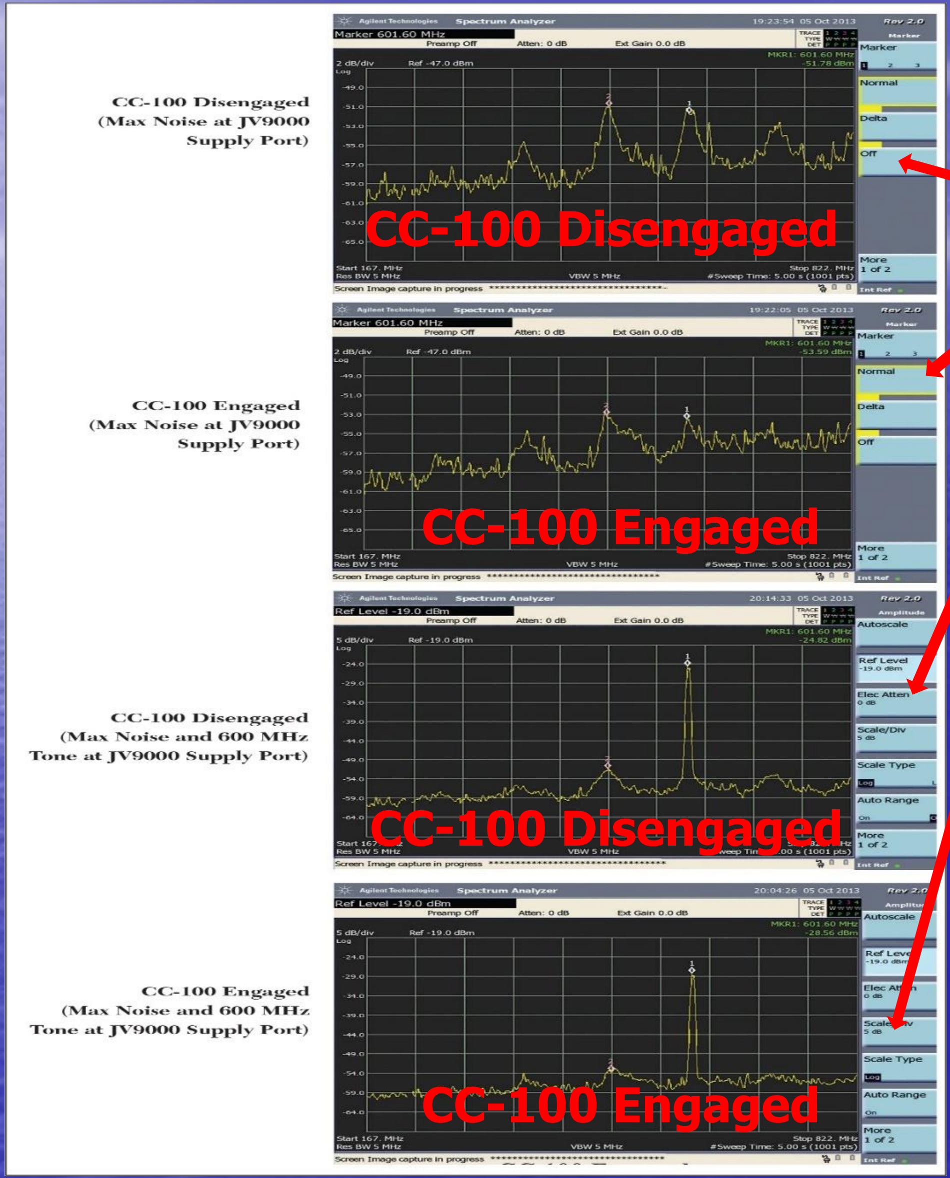
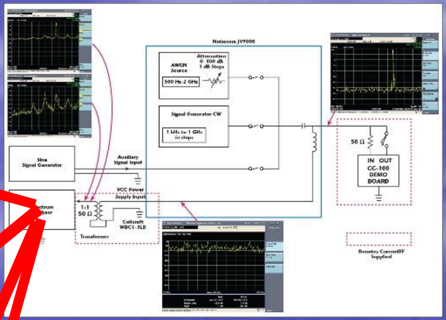


Figure 16a: CC-100 Disengaged

Figure 16b: CC-100 Engaged

CC-100 PowerOp Device Spectral Response, Power Grid Compensation, and EMI Suppression





JV9000/AT-N1996A Test/Measurement System

EMI Suppression due to CC-100 Negative Feedback

(spectral smoothing effects of the CC-100 Engaged plots)

Conclusions/Take-Aways

- The PowerStic,Exodus, and CC-100 recovers and saves up to 20% of Circuit Dynamic Power in Application configurations.
- The CC-100 recovers and saves power at the System, PCB, and IC levels of integration with little interaction between Integration levels.
- The CC-100 possesses an Ultra-Low input impedance as evidenced by device S11 plots.
- The CC-100 possesses a 300Mhz to 1.6Ghz effective bandwidth.
- Due to the negative feedback action of the CC-100, the device aids in power integrity/transient and EMI suppression in system power grids.
- "Real World" circuit noise sources are typically intermittent and variable, thus test runs "with" and "without" the CC-100 and derivatives using these intermittent sources must be averaged to produce reliable test measurement results

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