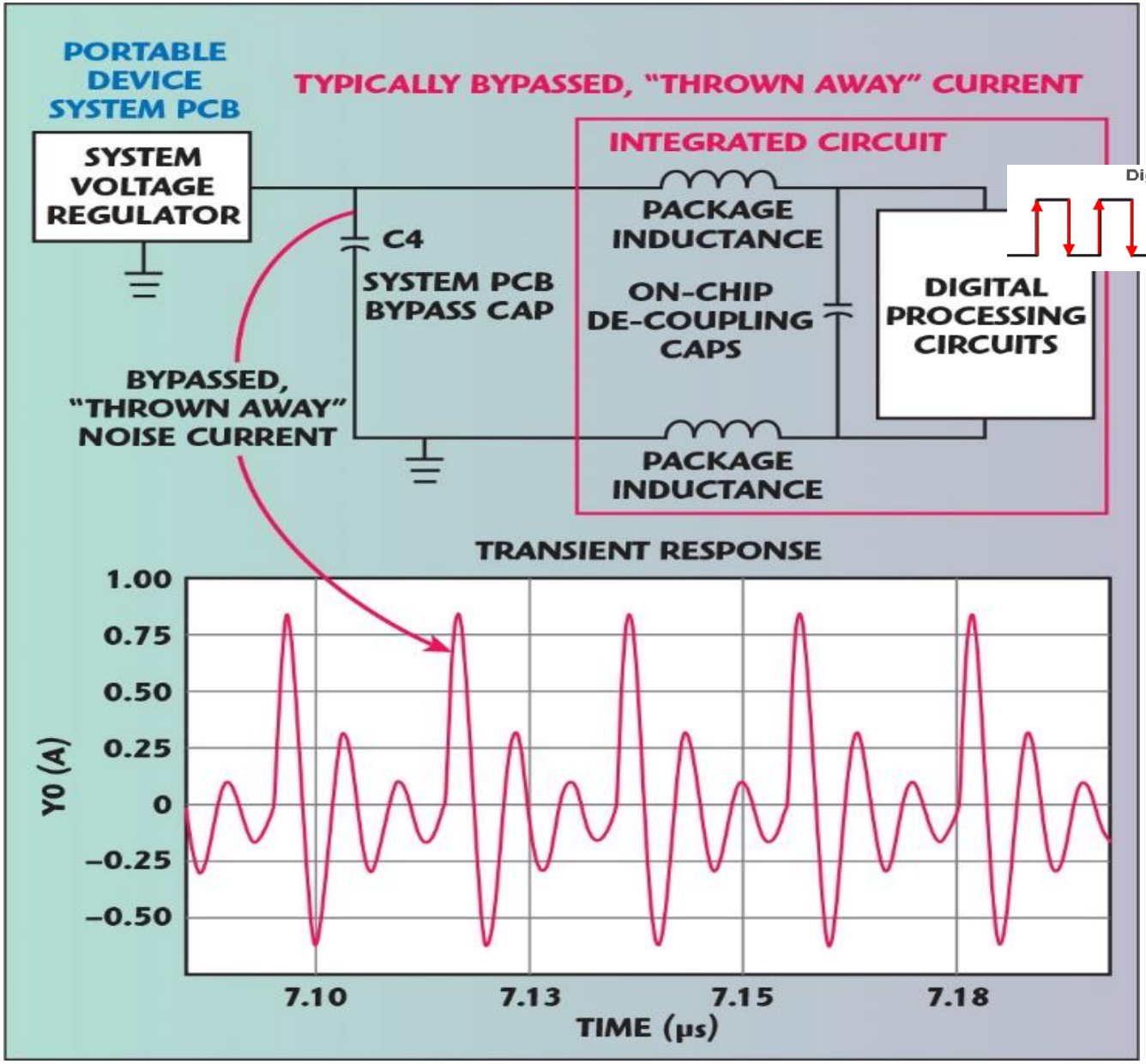
CurrentRF CC-100 Power Optimizer Integrated Circuit

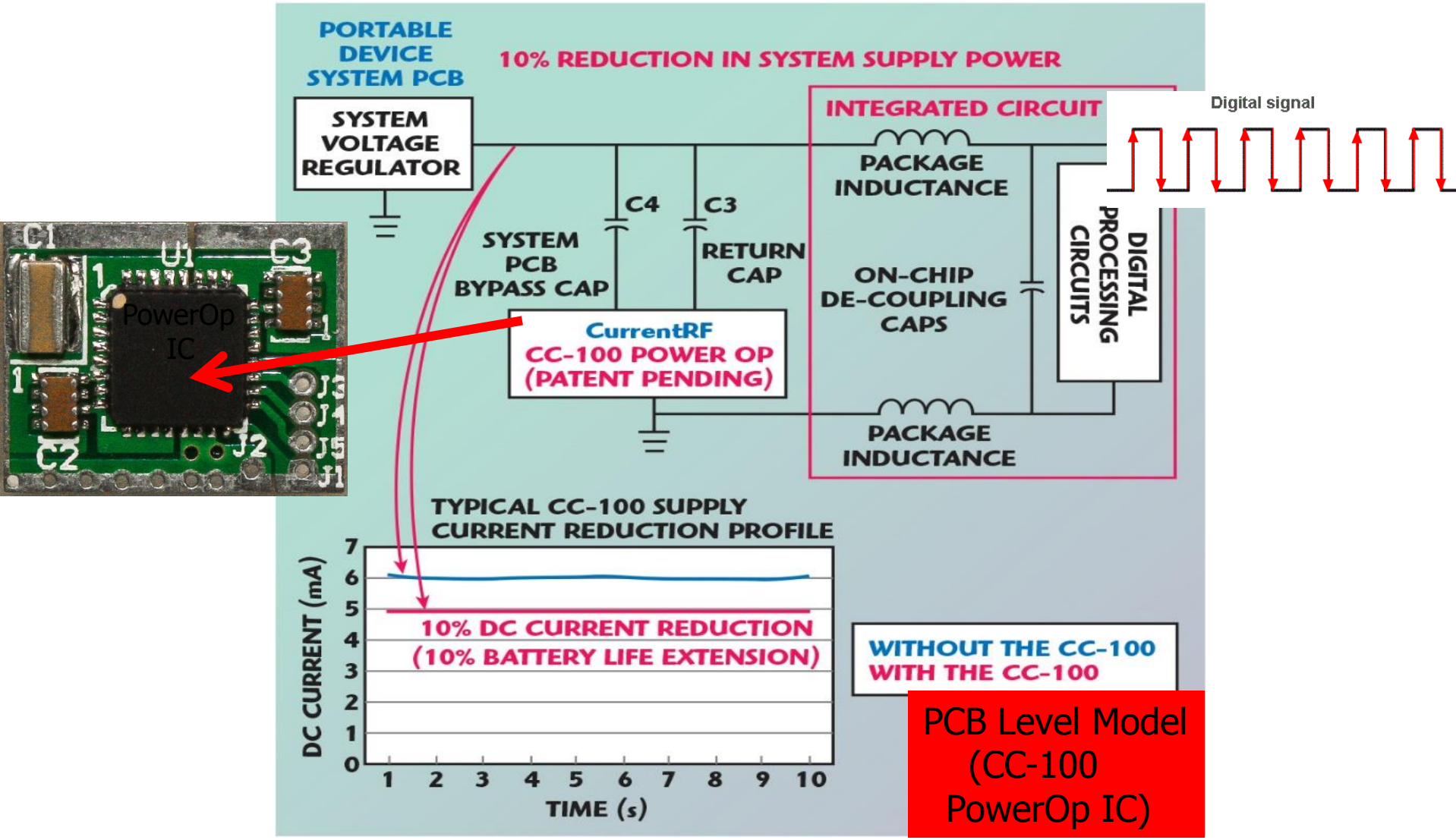
Recycle and Reuse “Throw-Away” System Circuit Noise Current with

the CC-100 IC

The Problem —Thrown Away, Unreachable System Noise Energy

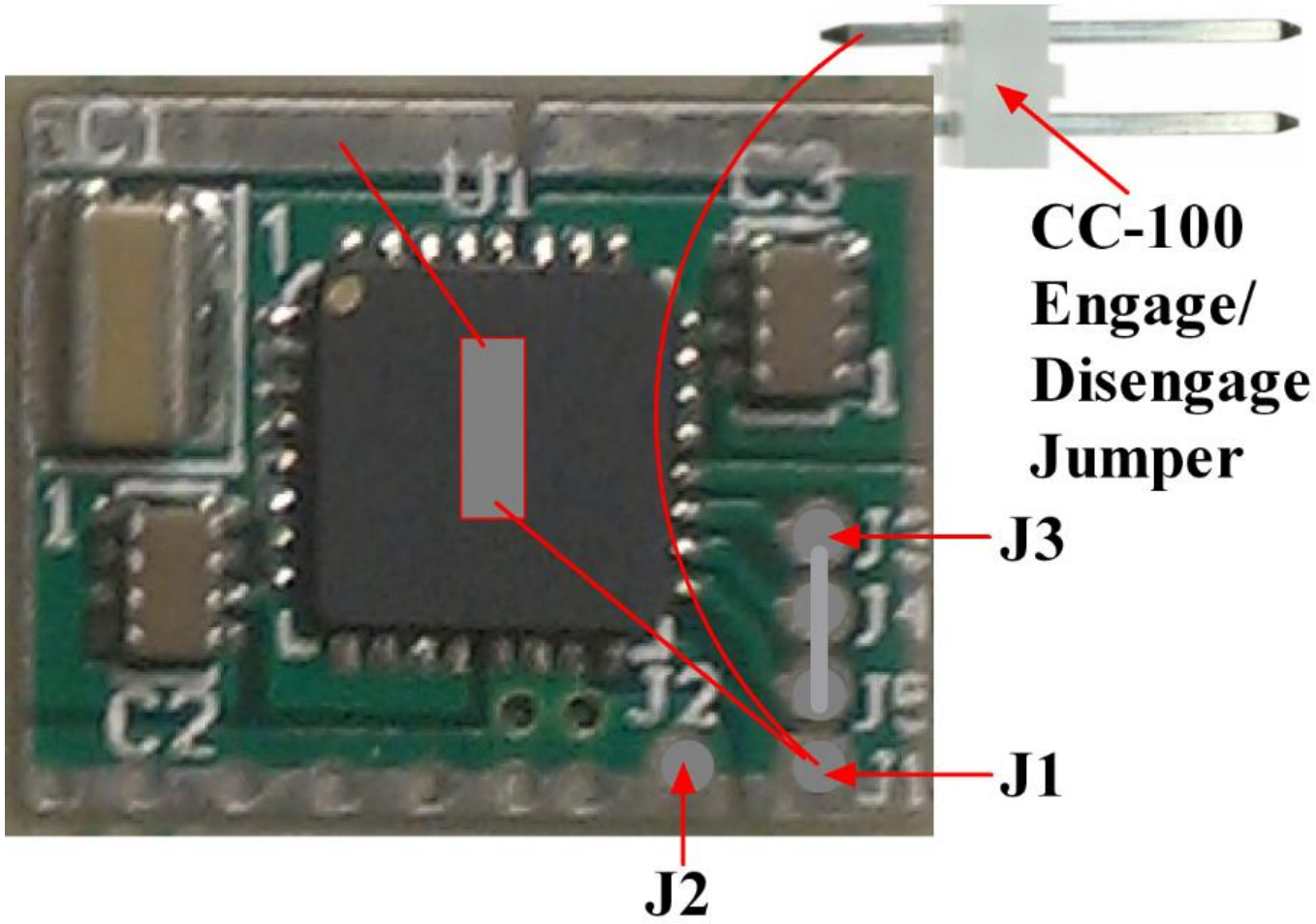


The Solution: The CC-100 Power Optimizer(PowerOp IC) Harvesting and Extracting Previously Unreachable Power at the PCB Level

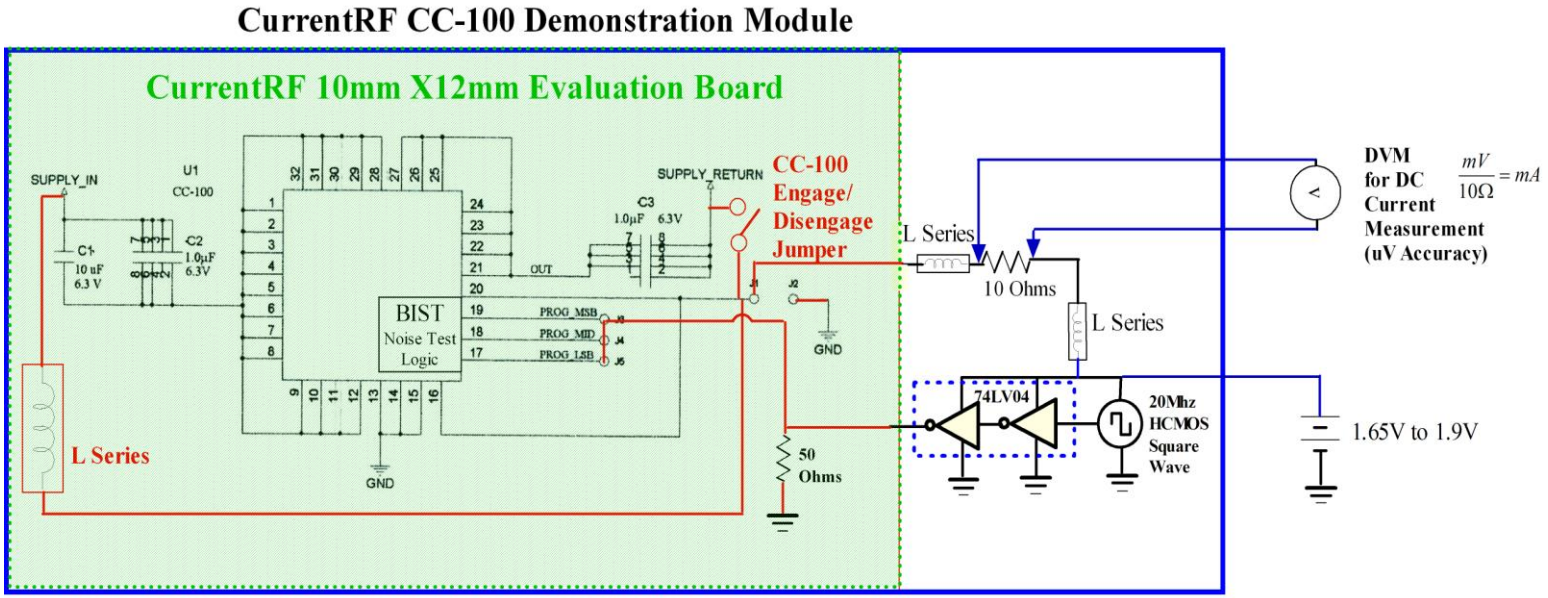


CC-100 Performance Tests

CC-100 IC Evaluation Module Test Circuit
5% to 24% Dynamic Current Reduction with Internal BIST Engine

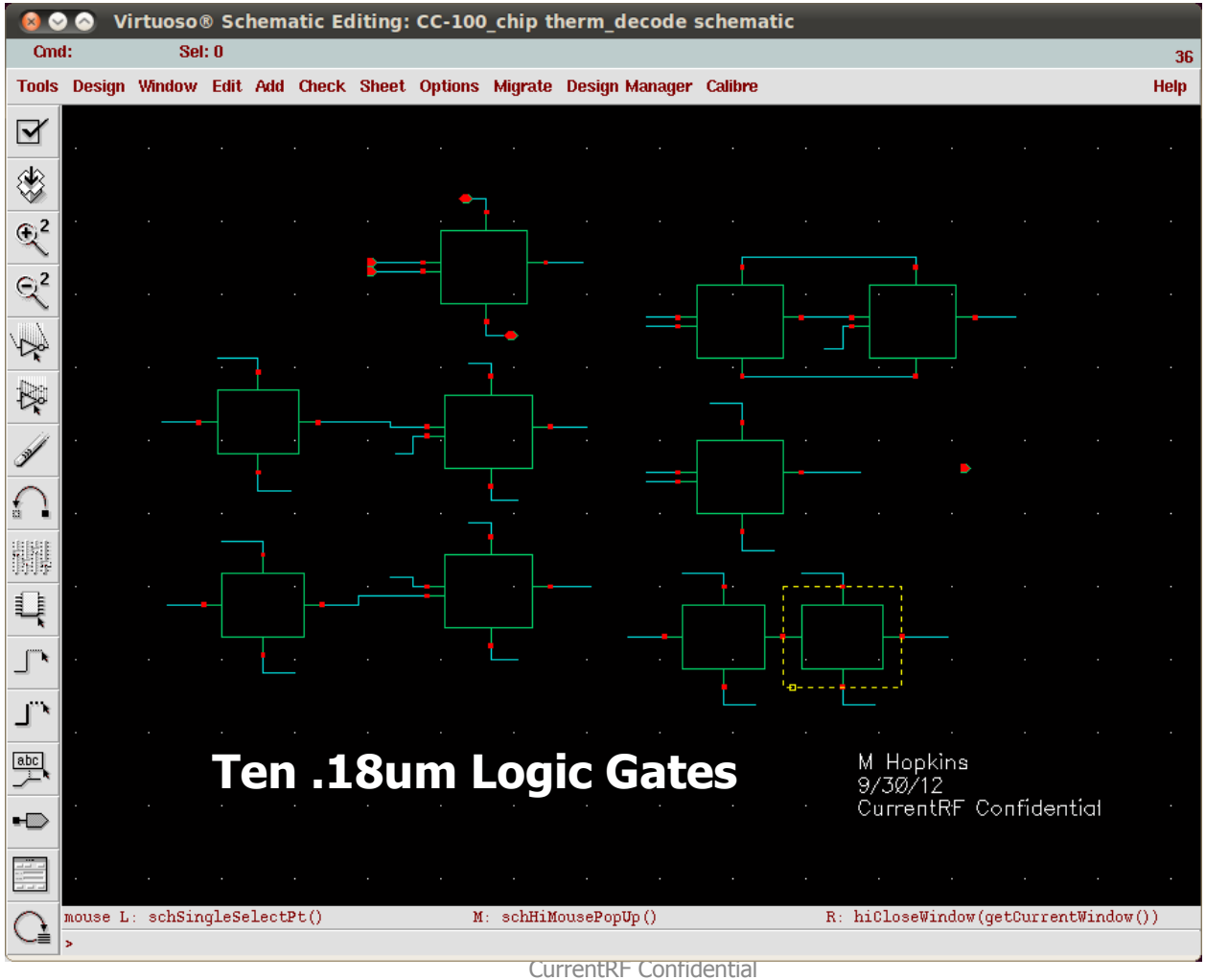


CC-100 IC Instantaneous Current Reduction
5% to 24% Dynamic Current Reduction with Internal BIST Engine



BIST Noise Test Logic=10 Logic gates(And, Or, Inverters)
Typical Metrics:
Supply Current- CC-100 Disengaged------> 4.249mA
Supply Current- CC-100 Engaged---------->3.774mA
Delta---------->.475mA
Percent Reduction---------->5%to 24%
Clock Rate---------->20 Mhz
Supply Voltage---------->1.65 V to 1.9V

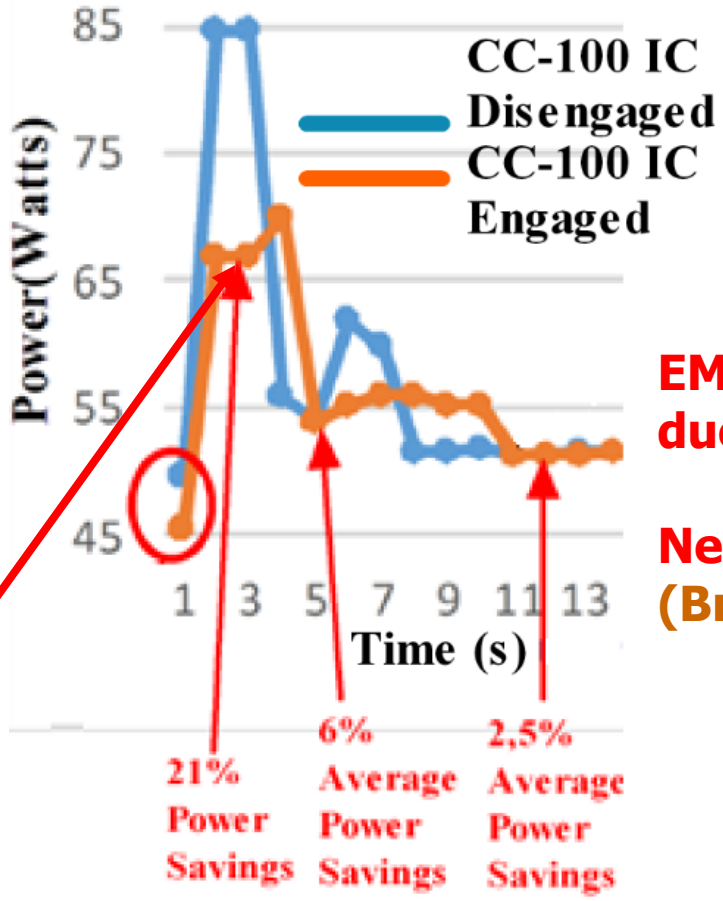
CC-100 IC Instantaneous Current Reduction
5% to 24% Dynamic Current Reduction with Internal BIST Engine



CC-100 IC Instantaneous Current Reduction
5% to 24% Dynamic Current Reduction with Internal BIST Engine

Supply Voltage (V)	CC-100 Engaged (mA)	CC-100 Disengaged (mA)	delta (mA)	Percentage Reduction
1.9	5.392	5.88	0.488	8.3
1.85	4.932	5.233	0.301	5.7
1.8	3.774	4.249	0.475	11.17
1.75	2.717	2,858	0.141	5
1.7	1.997	2.113	0.116	5.5
1.65	1.106	1.464	0.358	24.4
				(Average) 9.8

CC-100 IC Instantaneous Current Reduction
21% Power Reduction—149mA Current Reduction



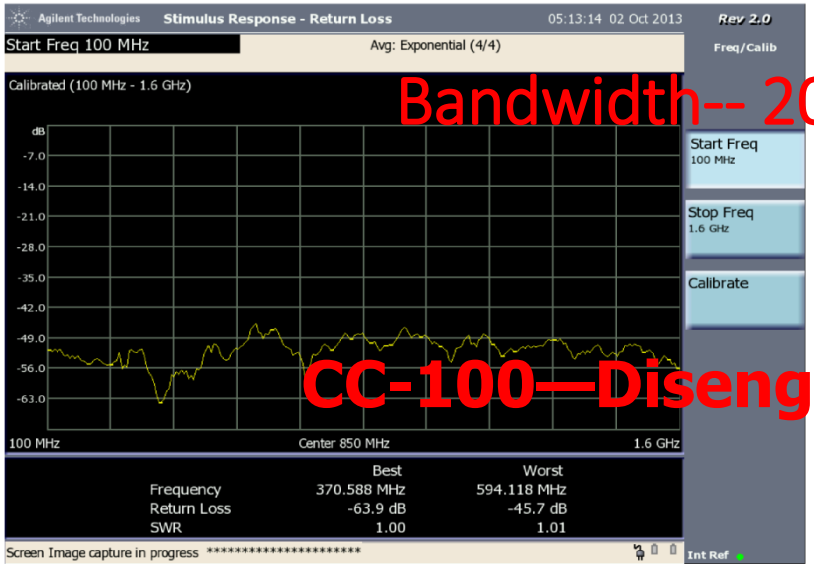
149 mA Current Reduction With the CC-100 Engaged

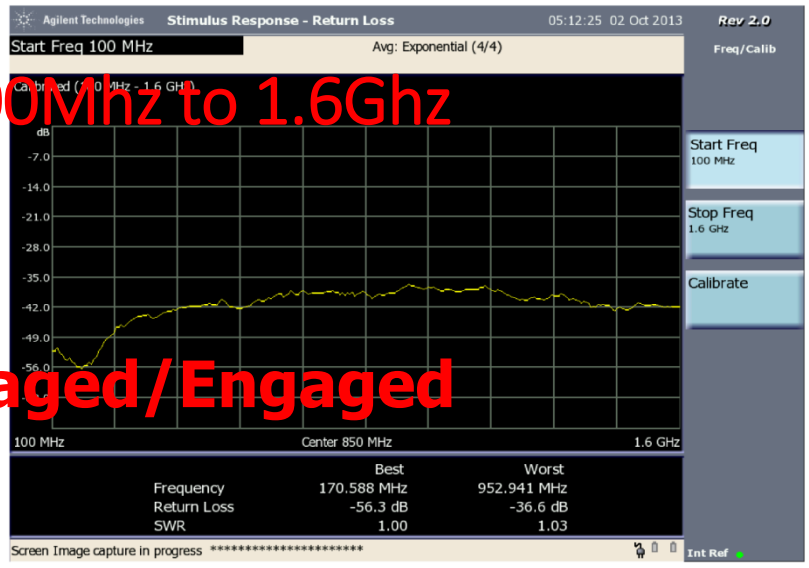
EMI Suppression due to CC-100 IC/IP Negative Feedback (Brown Trace)

CC-100 Input Impedance/Bandwidth Characterization

CC-100 PowerOp Device Input Impedance/Spectral Response

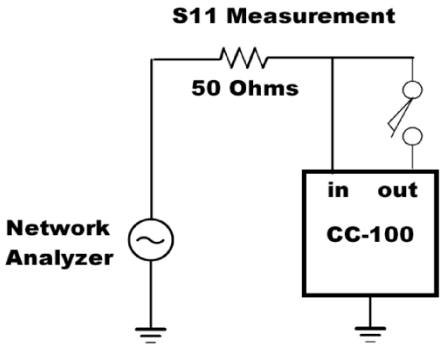
(Agilent AT-N1996A Network/Spectrum Analyzer)





Bandwidth-- 200Mhz to 1.6Ghz

CC-100—Disengaged/Engaged



EMI Suppression due to CC-100 Negative Feedback

(spectral smoothing effects of the CC-100 Engaged plot)

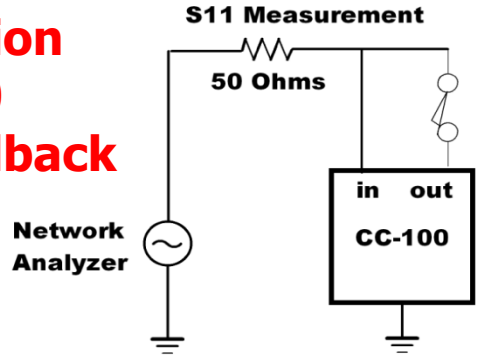


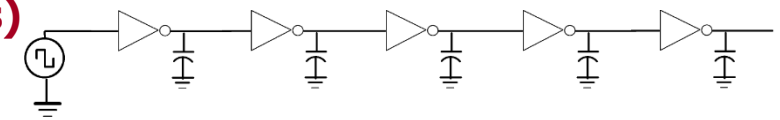
Figure 16a: CC-100 Disengaged

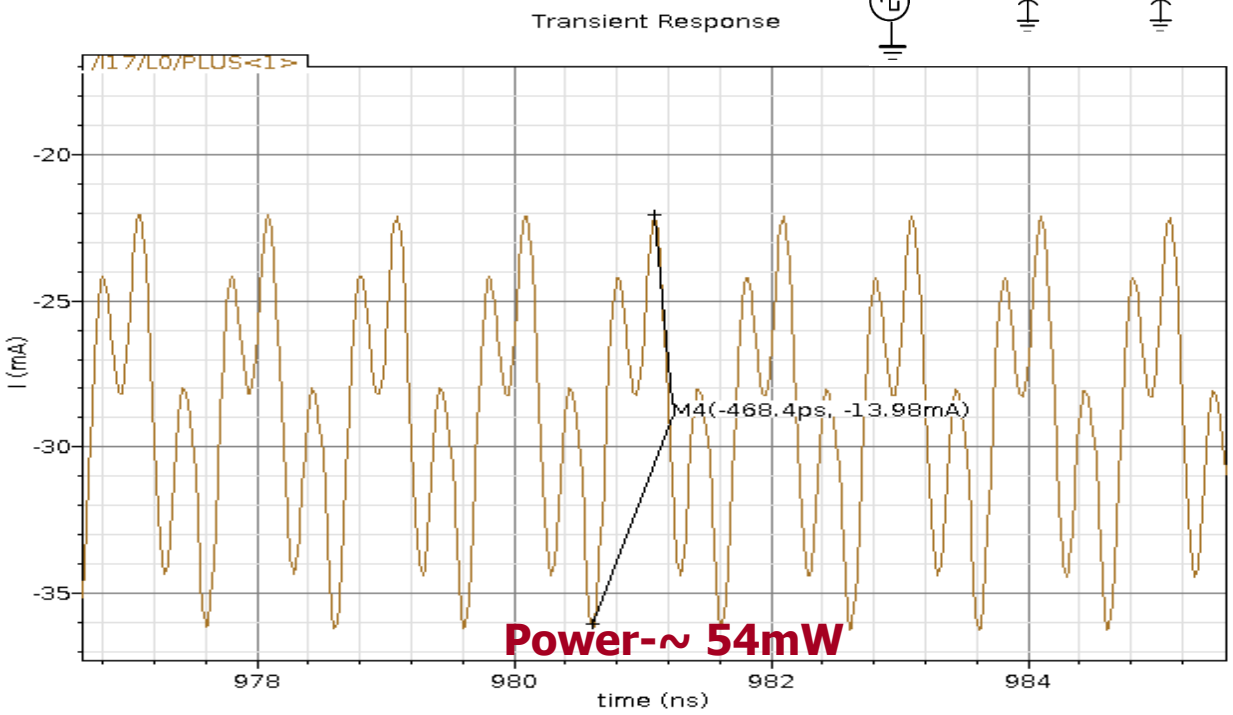
Figure 16b: CC-100 Engaged

CC-100 IC Simulation vs Silicon Correlation

Supply Current Simulation With the CC-100 Disengaged (1Ghz Clocks-High Noise)

Simple Inverter Chain running at 1Ghz without the CC-100 (250ps logic edges)

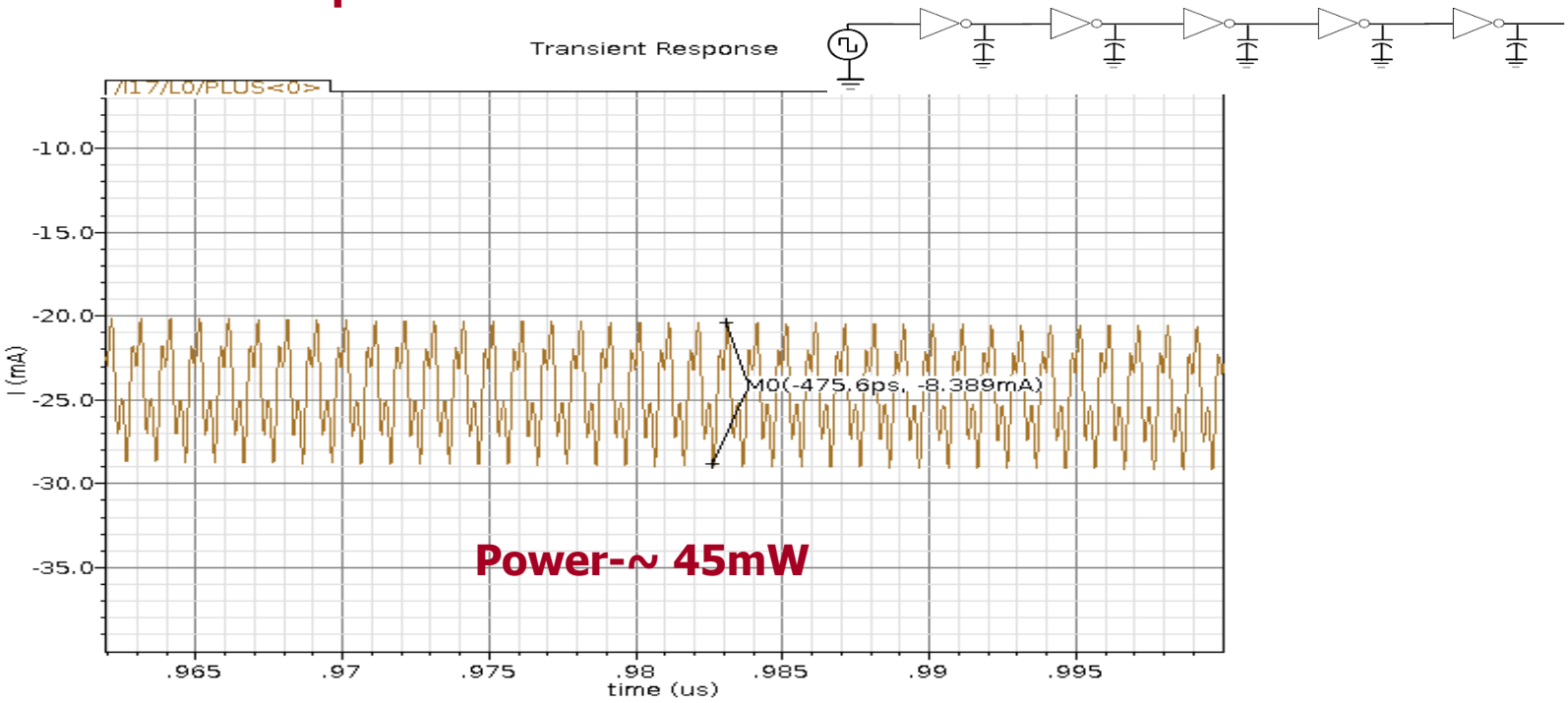




Power-~ 54mW

Reduced Supply Current Simulation with the CC-100 Engaged

Simple Inverter Chain running at 1Ghz
with the CC-100
AC Peak to Peak Current Reduction-40%
Total Composite AC and DC Current Reduction-15%

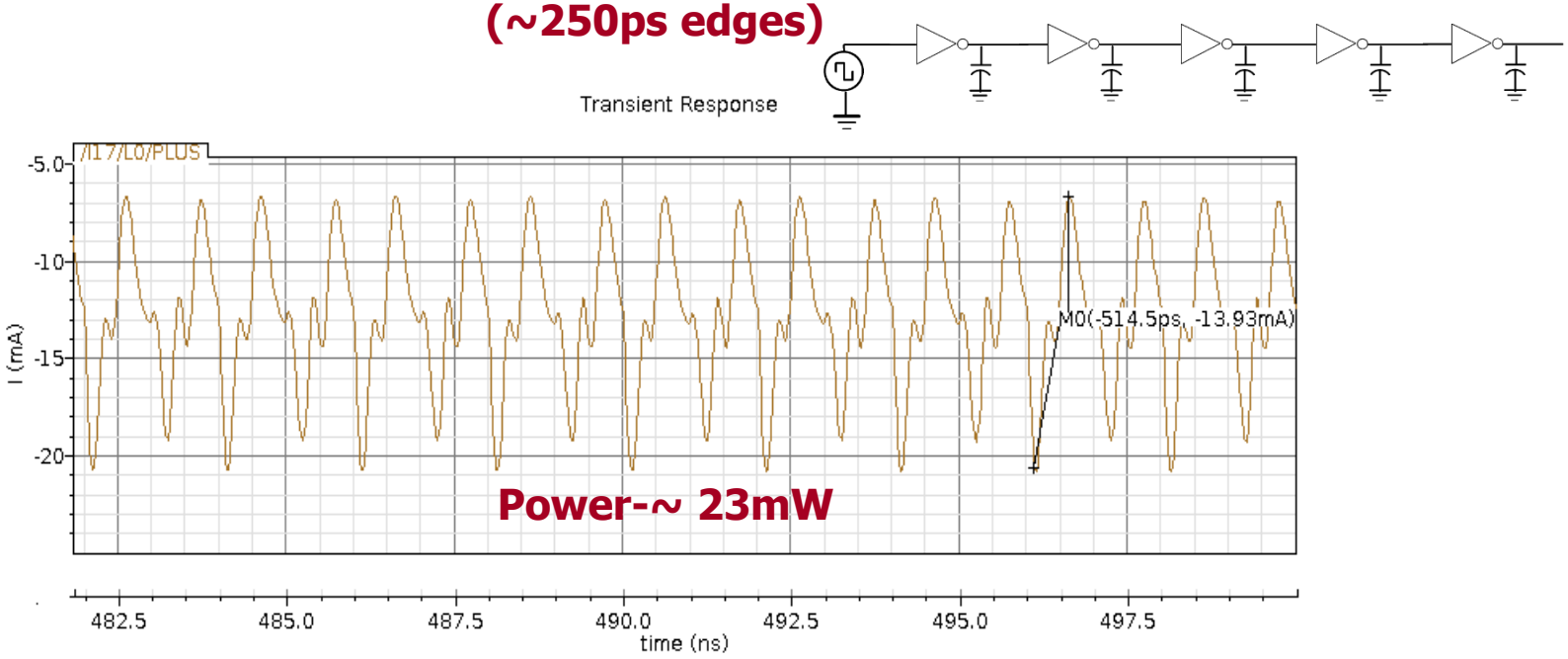


Power-~ 45mW

Current Reduction-~5mA
Total Power Reduction(1.8V supply)-~9mW

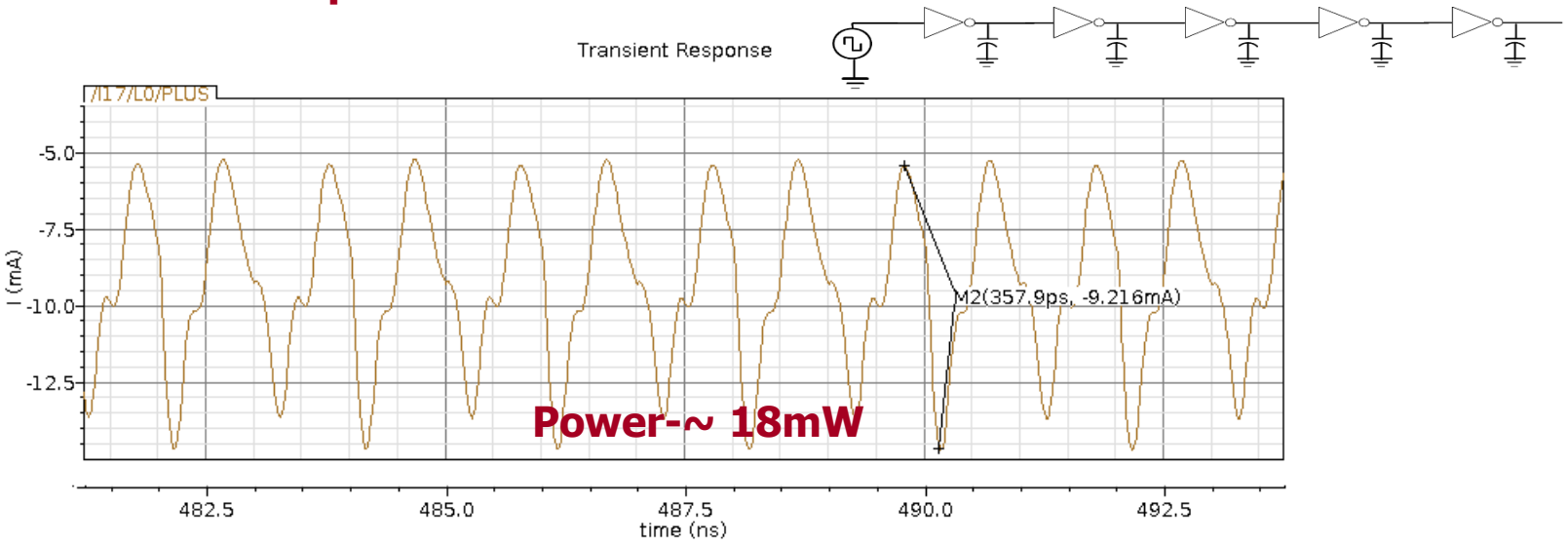
Supply Current Simulation With the CC-100 Disengaged (500Mhz Clocks-High Noise)

Simple Inverter Chain running at 500Mhz without the CC-100 (~250ps edges)



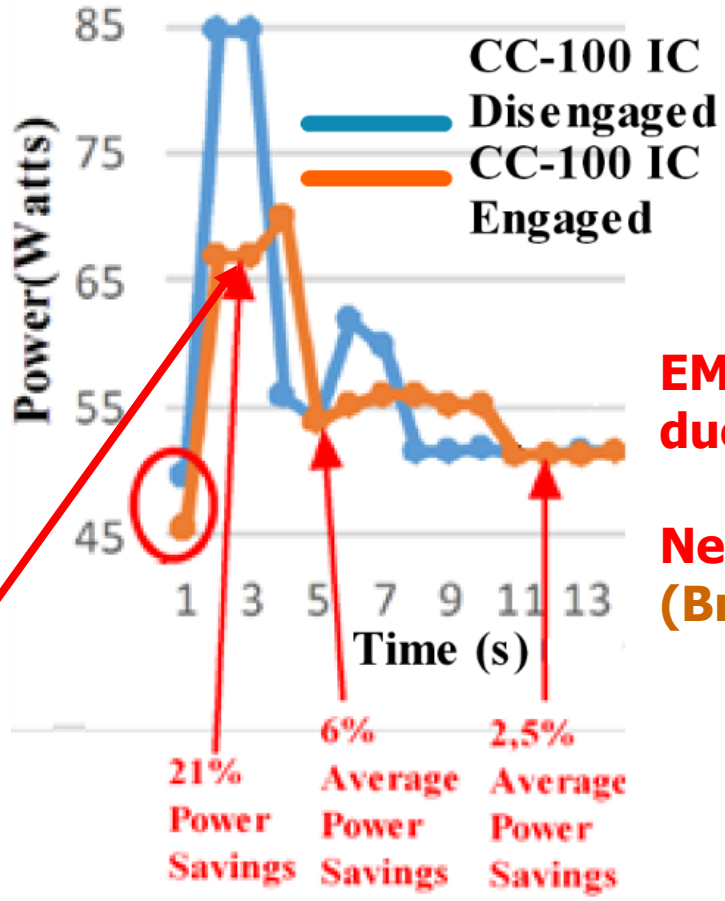
Supply Current Simulation With the CC-100 Engaged (500Mhz Clocks-High Noise)

Simple Inverter Chain running at 500Mhz with the CC-100
AC Peak to Peak Current Reduction-34%
Total Composite AC and DC Current Reduction-27%



Current Reduction-~3mA
Total Power Reduction(1.8V supply)-~5mW

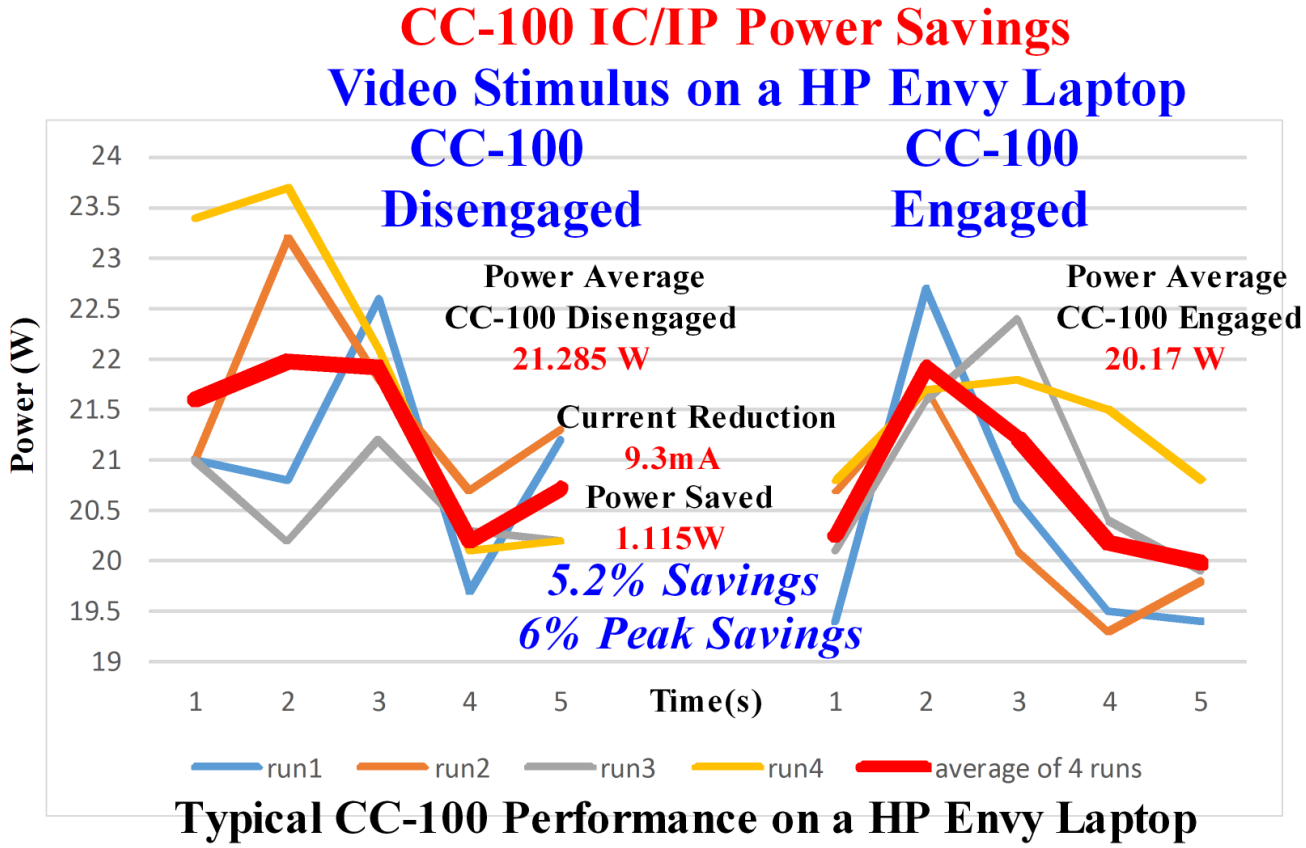
CC-100 IC Instantaneous Current Reduction
21% Power Reduction—149mA Current Reduction
Characterization Data



149 mA Current Reduction With the CC-100 Engaged

EMI Suppression due to CC-100 IC/IP Negative Feedback (Brown Trace)

CC-100 IC Current Reduction
5.2% Power Reduction--9.3mA Current Reduction
Characterization Data



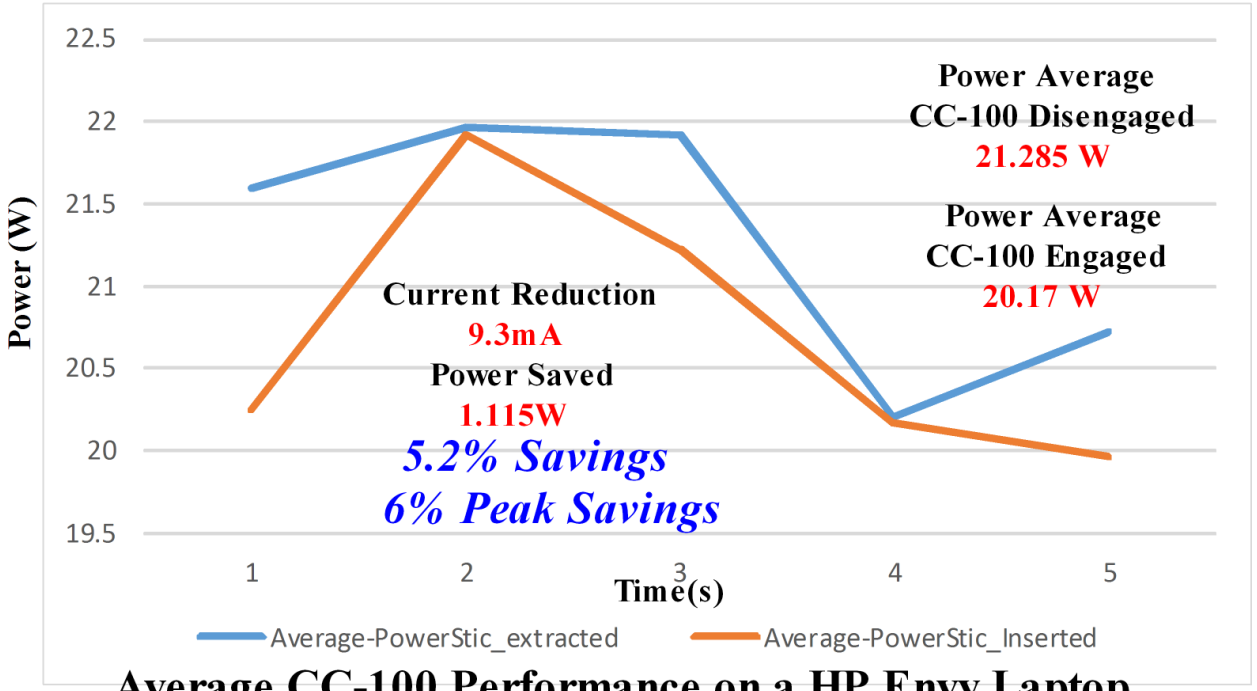
Typical CC-100 Performance on a HP Envy Laptop

9.3 mA Average Current Reduction With the CC-100 Engaged

EMI Suppression due to CC-100 IC/IP Negative Feedback

CC-100 IC Average Current Reduction
5.2% Power Reduction--9.3mA Average Current Reduction
Characterization Data

CC-100 IC/IP Average Power Savings
Video Stimulus on a HP Envy Laptop



Average CC-100 Performance on a HP Envy Laptop

9.3 mA Average Current Reduction With the CC-100 Engaged

CC-100 Demonstration Board Tests

The CC-100 Engaged/Disengaged Characterization Data

Number of Active LSFRs	The CC-100 PowerOp IC Inserted (DC mA)	The CC-100 PowerOp IC Extracted (DC mA)	Supply Current Reduction (DC mA)	Percentage Dynamic Current Reduction
9	164.7	174.1	9.4	5.4
8	147.2	154.1	6.9	4.47
7	129	134.4	5.4	4
6	111.4	116	4.6	3.9
5	93	96.7	3.7	3.8
4	74.6	77.6	3	3.8
3	56.4	58.2	1.8	3.1
2	37.7	39	1.3	3.3
1	19.1	19.8	0.7	3.5

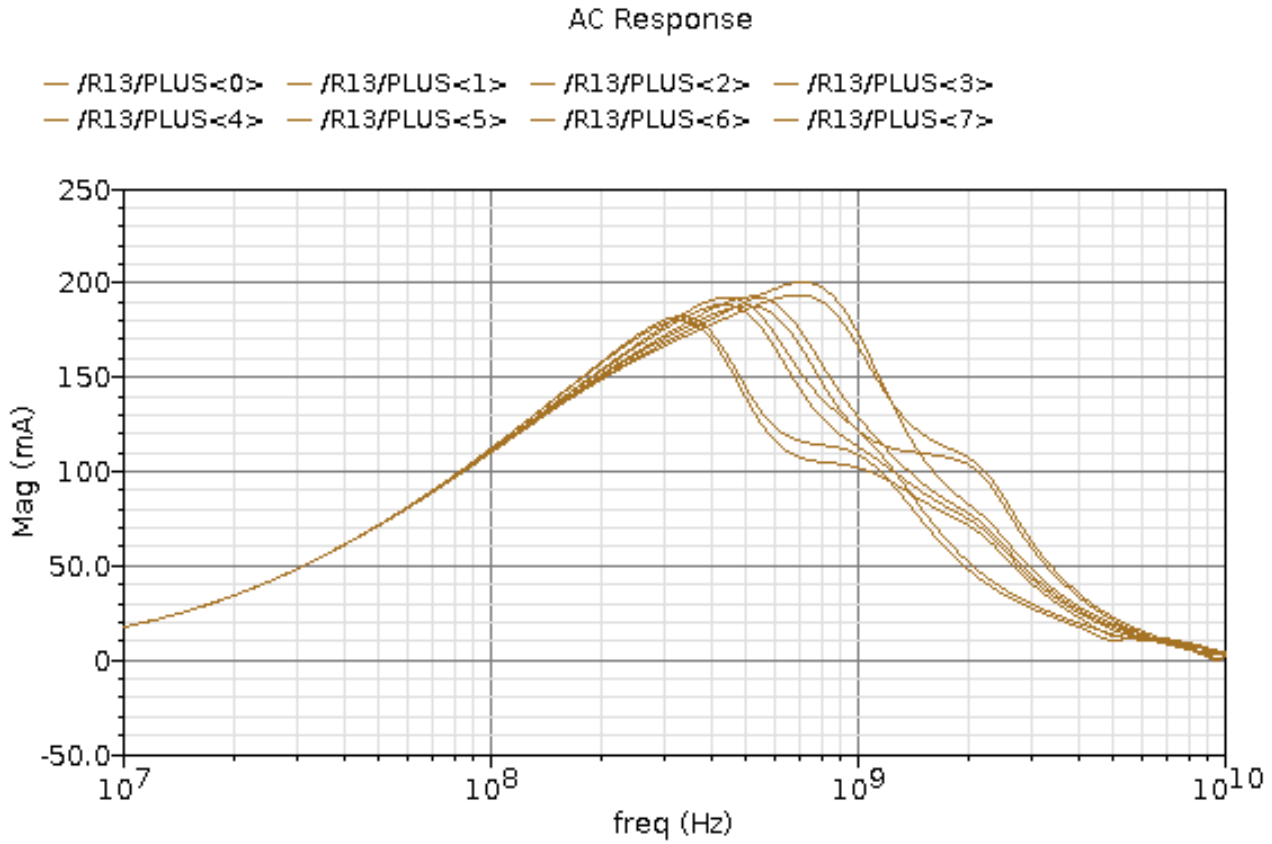
CC-100 Average Savings→ 13uA/Mhz

CC-100 IC Instantaneous Current Reduction
5% to 24% Dynamic Current Reduction with Internal BIST Engine
(Ten .18um Logic Gates running at a 20Mhz Rate)
IC Power Reduction Performance

Supply Voltage (V)	CC-100 Engaged (mA)	CC-100 Disengaged (mA)	delta (mA)	Percentage Reduction
1.9	5.392	5.88	0.488	8.3
1.85	4.932	5.233	0.301	5.7
1.8	3.774	4.249	0.475	11.17
1.75	2.717	2,858	0.141	5
1.7	1.997	2.113	0.116	5.5
1.65	1.106	1.464	0.358	24.4
				(Average) 9.8

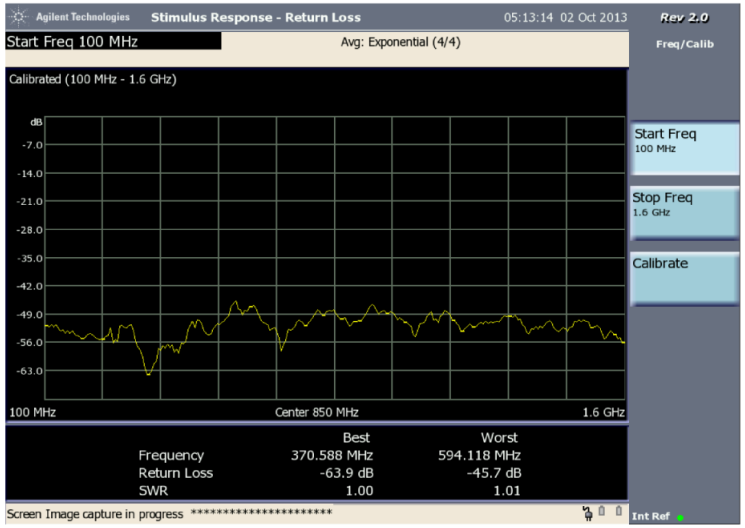
CC-100 IC Frequency/Magnitude Response

CC-100 IC Simulated Frequency Response



CC-100 IC Measured Frequency Response

Characterization Data



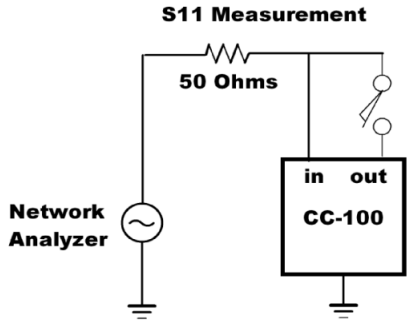
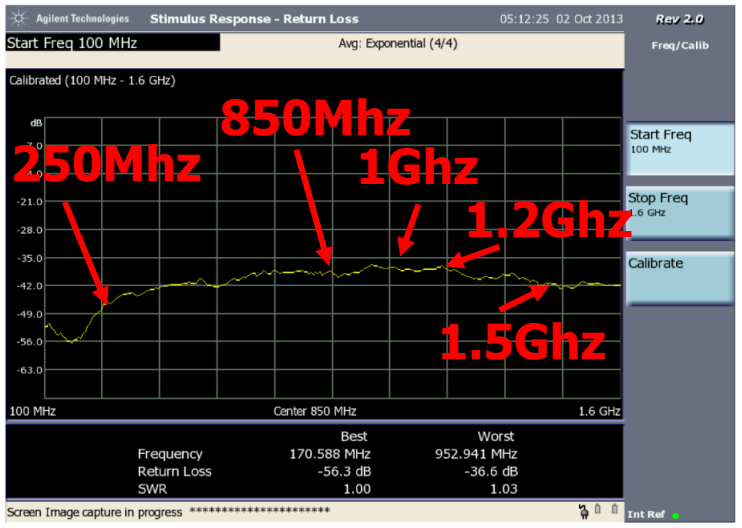


Figure 16a: CC-100 Disengaged



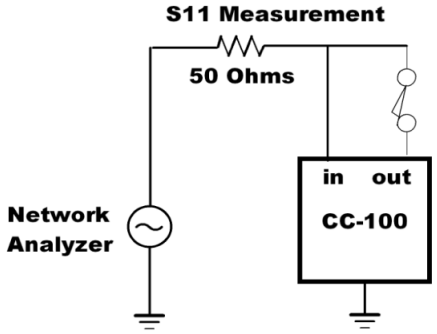


Figure 16b: CC-100 Engaged

CC-100 IC Simulation vs Silicon Predictive Capability

CC 100 IC Predictive Simulation Procedure

CurrentRF has developed the capability of accurate estimate and prediction of CC-100 IC power savings in your IC design.

Prior to CurrentRF IC engagement, do the following:

1) simulate one of your digital blocks.

2) keep the dynamic supply currents of the above simulation.

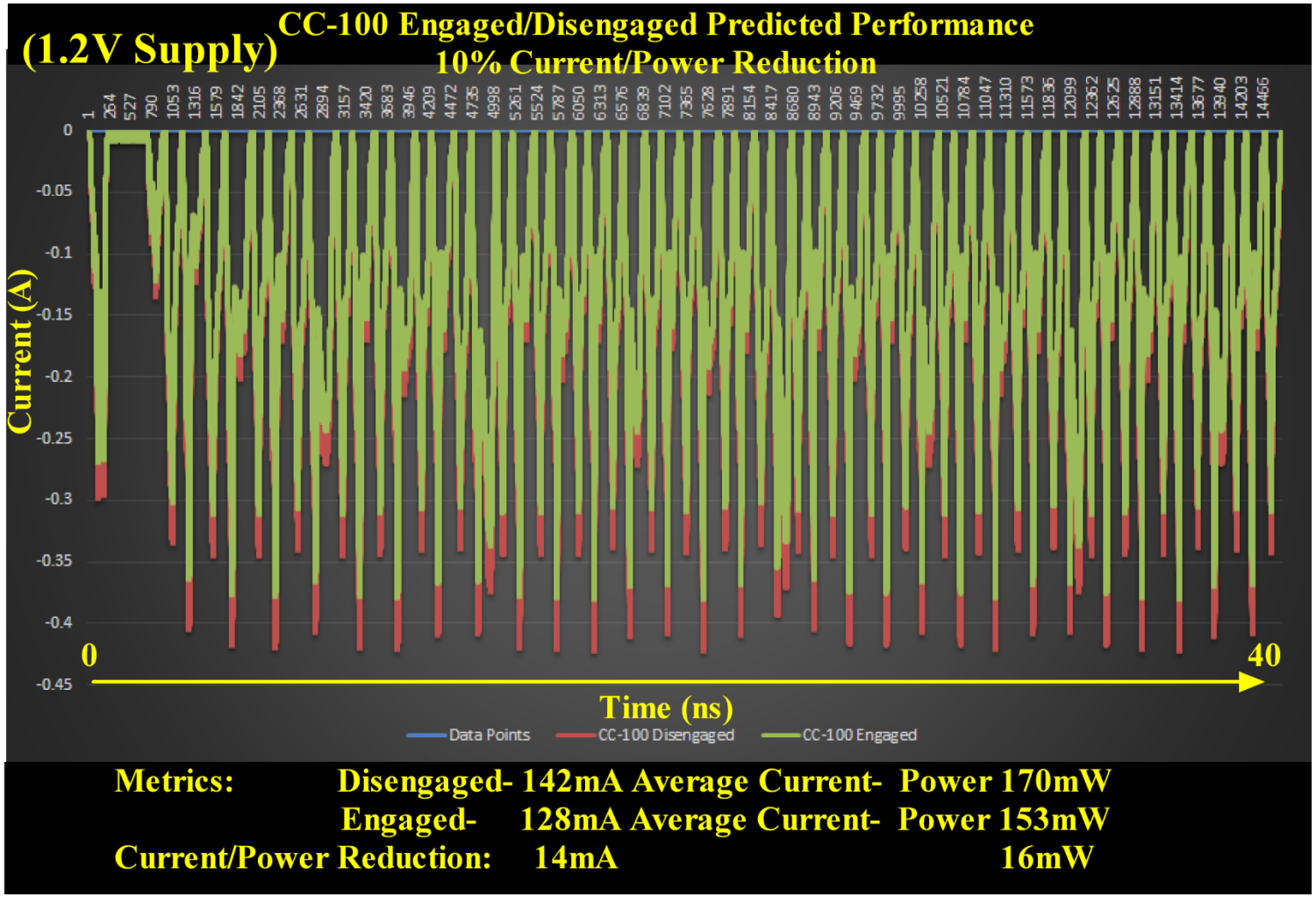
3) send them to us in an excel spreadsheet format(time vs. supply current magnitude).

We do not need to know the circuit details of your design, just the magnitude of the current draw per unit time from your behavioral supply in your simulations.

With this information, we can predict the current and power savings you will see in your system by including the CC-100 IC in your design, and will share them with you.

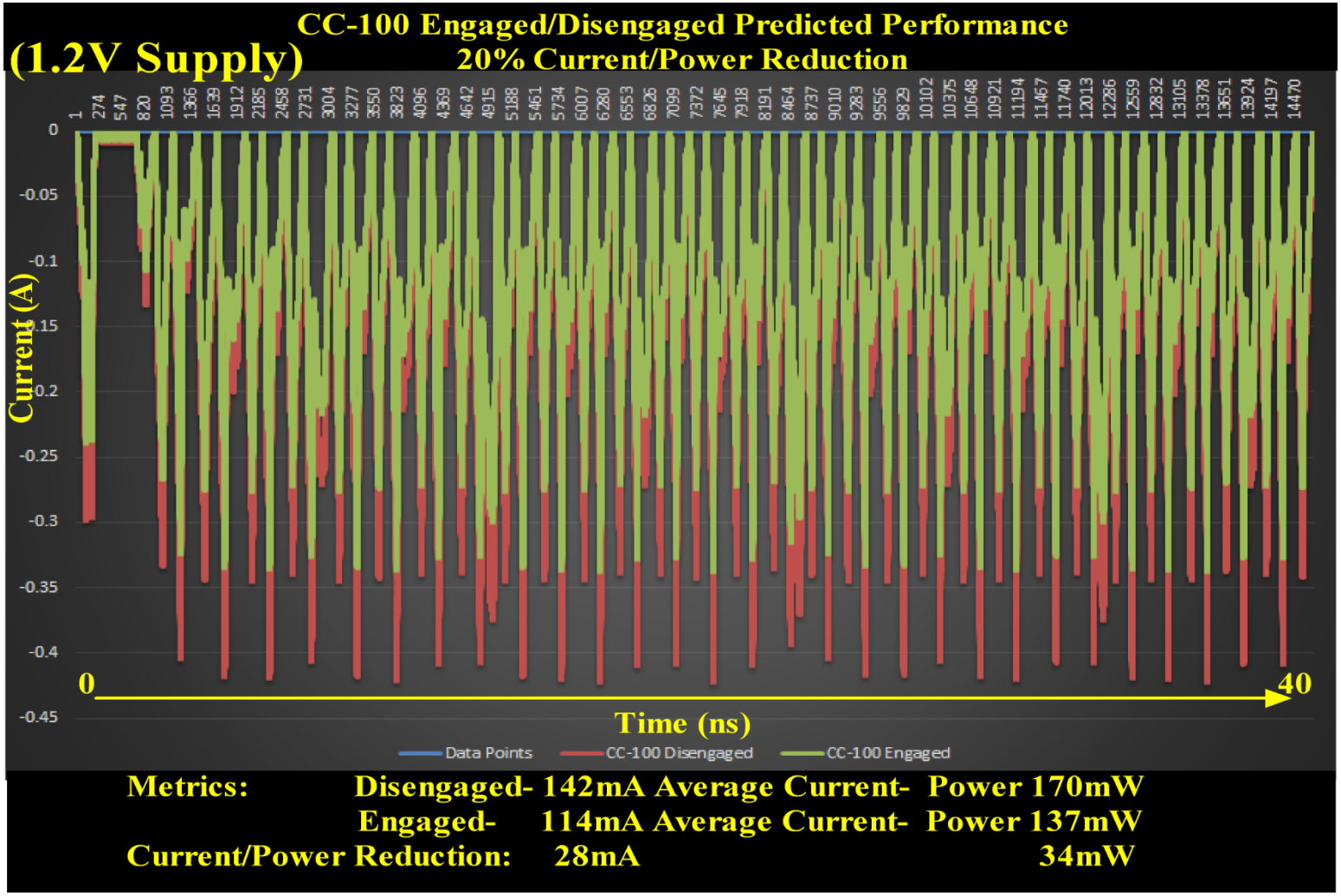
Example results of the above methodology performed for other customers are shown in slides 39 through 41 of this presentation.

CC-100 IC Simulation vs Silicon Predictive Capability



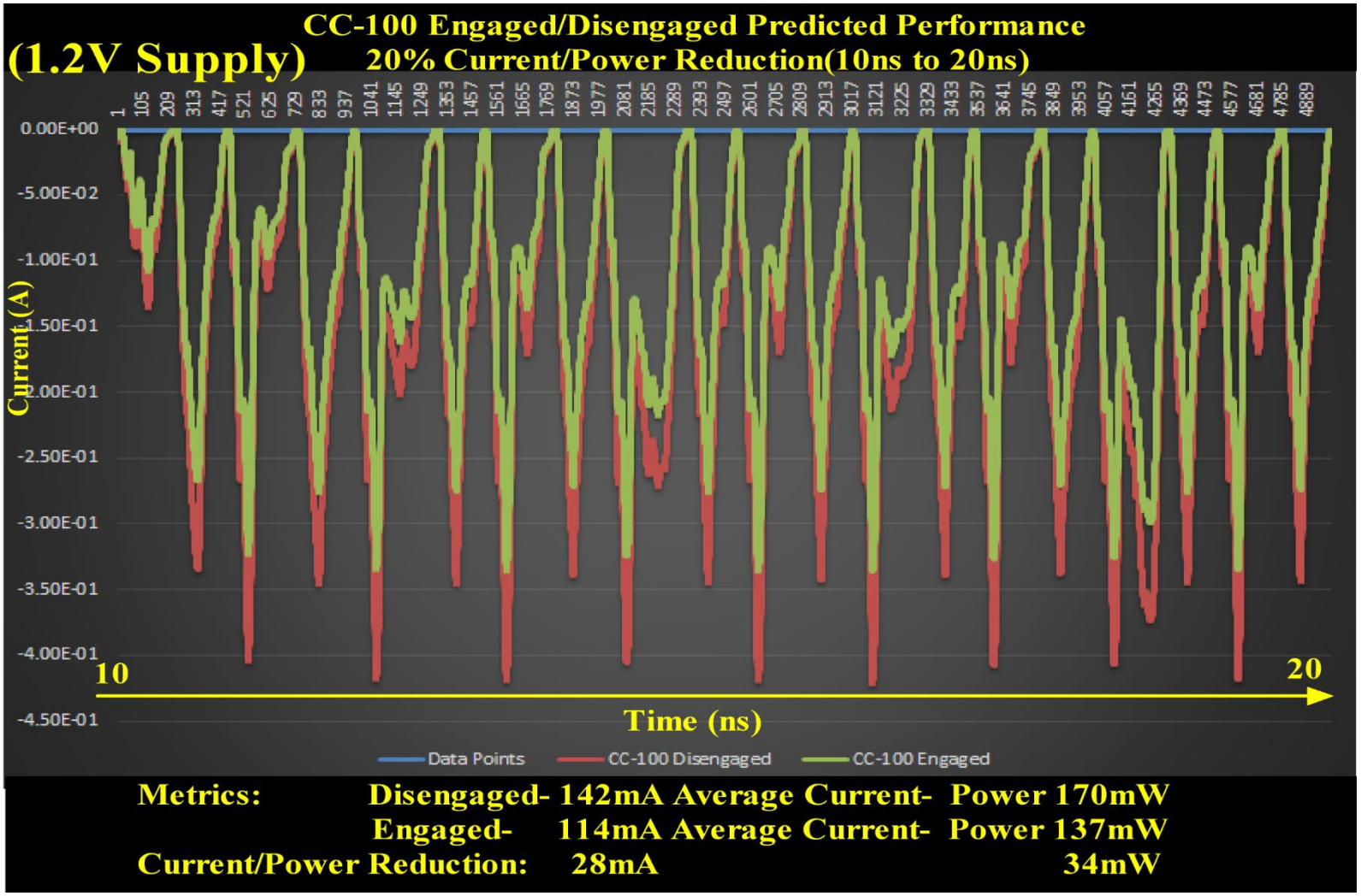
1Ghz Clock Driven DSP

CC-100 IC Simulation vs Silicon Predictive Capability



1Ghz Clock Driven DSP

CC-100 IC Simulation vs Silicon Predictive Capability



1Ghz Clock Driven DSP

Conclusions/Take-Aways

- The CC-100 IC recovers and saves up to 20% of Circuit Dynamic Power in Application configurations.
- The CC-100 IC design simulations and characterization data show good agreement, thus predictable simulation vs "real world" performance.
- The CC-100 IC performance in a given system can be predicted, given plots of the dynamic current drawn by system devices/circuits, from the system supply.
- The CC-100 IC activates when DSP/Digital Logic is active.
- The CC-100 IC can be used in conjunction with other power saving techniques.
- The CC-100 IC possesses an Ultra-Low input impedance as evidenced by device S11 plots.
- The CC-100 IC possesses a 200Mhz to 1.6Ghz effective bandwidth.
- Due to the negative feedback action of the CC-100, the IC aids in power integrity/transient and EMI suppression in system power grids.
- "Real World" circuit noise sources are typically intermittent and variable, thus test runs with the CC-100 IC Engaged and Disengaged using these intermittent sources must be averaged to produce reliable test measurement results

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