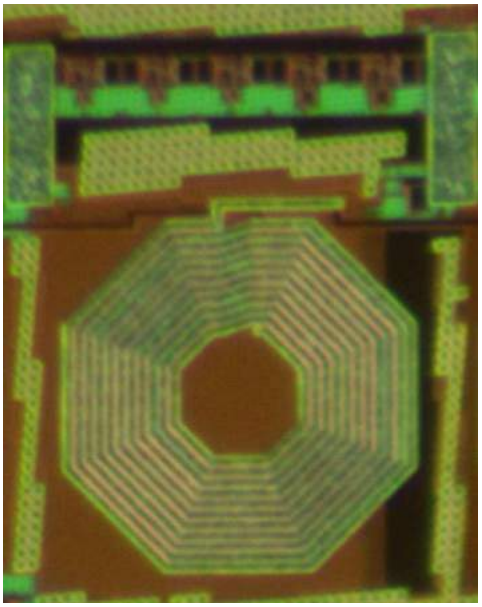
Current RF

CC-201IP and CC-202IP Revolutionary, Low Phase Noise, Single Ended to Differential Amplifier-LNA and Gain Blocks



Applications:

RFID
Wireless Power Transfer
Ultra-Low Noise, High Gain Amplifiers/LNAs
Eliminates needed Oscillator Overtone Operation
Fundamental, 3rd, and 5th order Oscillator Circuits
ADC Track and Hold Clock Drivers
Switched Capacitor Clock Drivers
PLL Wide-Band Spurious Frequency Reduction

Features:

RFID Compatible
Wireless Power Transfer Control
Ultra-low Classical Noise Amplifier
Selectable 2nd Order Bandwidth Adjustability
Harmonic and Bandwidth selectable output
Replaces PLLs with cleaner, lower power profile
Cascaded for increased gain and narrower BW
IP portable to any manufacturing process

CC-201IP and CC-202IP General Description

The CC-201IP is a revolutionary, ultra-low classical noise single cell amplifier IP block that possesses approximately 30 dB (see Figure 2) of signal

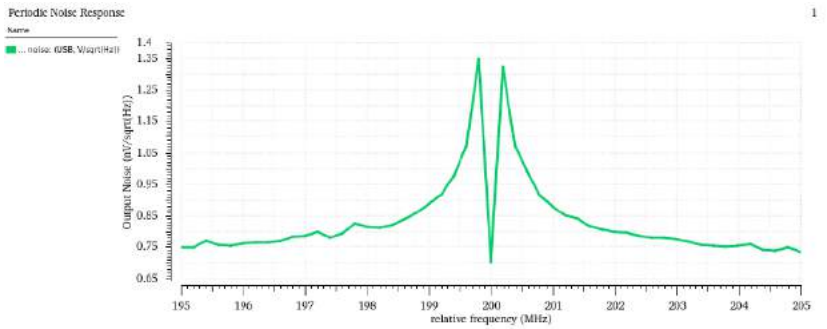


Figure 1: Single Cell Phase Noise with CML/CMOS Differential Clock Outputs

gain over a 200Mhz to 2.5Ghz adjustable bandwidth, while contributing only 1.3nV per root Hz (rms) of circuit phase noise (see Figure 1). As shown in Figures 2 and 6, the proprietary and patented design possesses a 2nd order bandpass function and is tunable from 50Mhz to 2.5Ghz(see Figures 1, 2, 5, and 6). The CC-201IP and CC-202IP blocks convert small signal, to amplified, differential, almost zero noise signals, the block is perfect for ultra-low noise, high gain, Low Noise Amplifiers (LNAs), ADC/Track and Hold Clock Generation, DAC Clock Generation, Clock Generation, DAC Clock Generation, Switched Capacitor Clock Generation and Distribution, and can be used for PLL output filtering to reduce wideband harmonics and spurious frequencies.

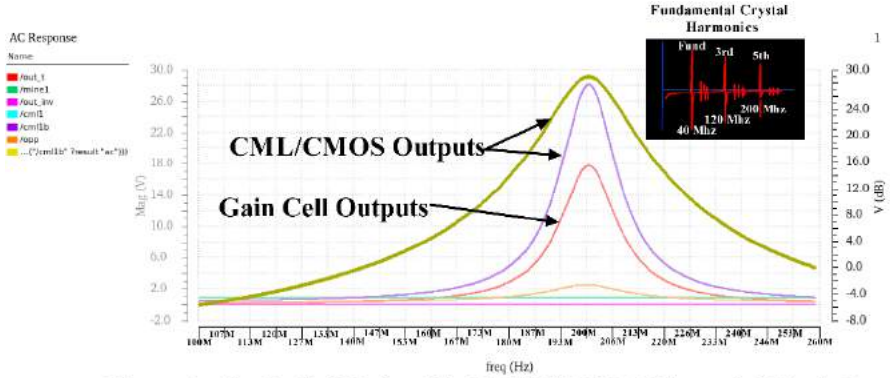


Figure 2: Single Cell Gain with CML/CMOS Differential Clock Outputs

As shown in the Figure 2 inset, the IP bock eliminates the need for Crystal Oscillator Overtone Operation since the IP can adjustably and selectively amplify the harmonics present in Crystal Oscillator outputs rejecting the fundamental and other generated harmonic frequencies present in Crystals, simplifying board level Crystal Oscillator support circuits. In the Figure 2 example, the CC-202IP frequency selection capabilities can effectively select the 120Mhz (3rd harmonic) or 200Mhz (5th harmonic) frequency and amplify, rejecting the 40 Mhz fundamental. The IP block can be adjusted to fit other frequency plans provided by lower fundamental frequency crystals and resonators.

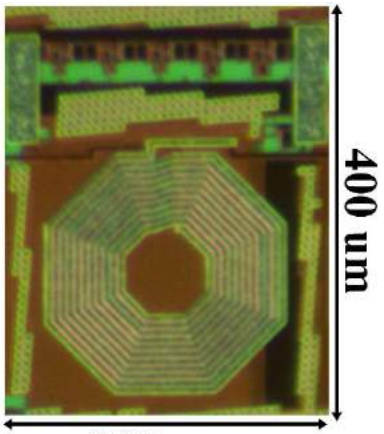


Figure 3: Example Cell Dimensions

Figure 3 shows the CC-201IP example cell dimensions. The inductor is sized for 100 to 200 Mhz operation and gets considerably smaller as operational frequencies increase. The CC-203IP (CurrentRF Super Inductor IP) can be utilized for further Inductor size reduction, On-chip Inductor Q enhancement, and CC-202IP frequency selectivity enhancement. All active circuits needed for the CC-202IP operation can fit underneath the central inductor, thus reducing the overall footprint of the IP. In the Figure 3 instance, the cell was taped out and characterized on Jazz Semiconductors SBC18HXL manufacturing process, and can easily be ported to any modern Bipolar or CMOS manufacturing process.

CC-202IP Cascaded RF Amplifier/LNA/Filter

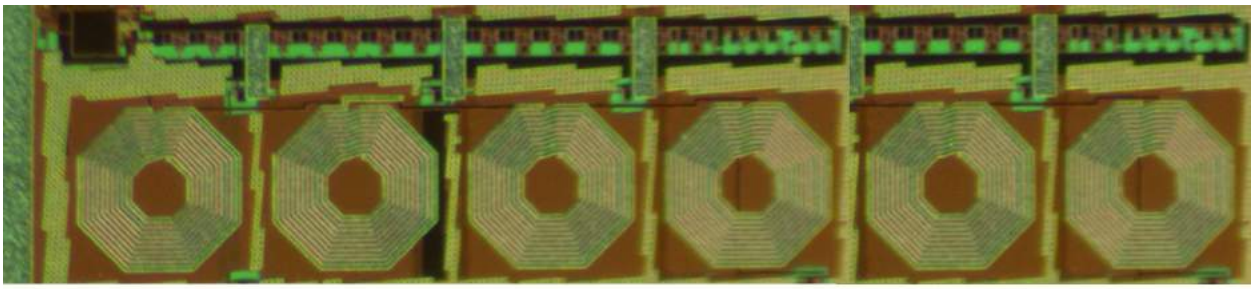


Figure 4: 6 Stage, Cascaded RF Amplifier/Filter

The CC-201IP Cell, shown in Figure 3, can be cascaded to form a multistage RF Amplifier/LNA/Filter, the CC-202IP, an example of this cascading shown in Figure 4. In this example, the total cumulative phase noise rises to 8nV per root Hz (rms), now centered at 2.5Ghz, as shown in Figure 5. The cell gain is shown to rise from approximately 30dB centered at 200Mhz for the single gain and CML/CMOS cell, (the CC-201IP), shown in Figure 3, to nearly 70dB (the CC-202IP) centered at 2.5Ghz as shown in the cumulative plot of Figure 6.

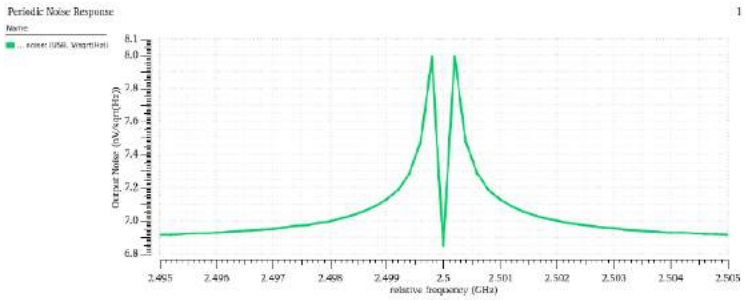


Figure 5: Cumulative Phase Noise of 6 Cascaded Stages with CML/CMOS Level Outputs

Both the single cell CC-201IP plot of Figure 2 and the multi-stage CC-202IP plot of Figure 6 feature outputs with signal swings ranging from high CML to CMOS signal levels. Shown in Figure 2, the sensitivity of the CC-201IP and the gain of the CML/CMOS cell is 28mV rms or 80mV pp, creating an output SNR of -171dBc, which makes the CC-201IP perfectly suitable for single stage LNA applications, the amplification of off-chip, clock crystal or resonator fundamental or odd order signal magnitudes for clean clock ADC, DAC , Track and Hold, and ultra-low noise switched capacitor applications. In Figure 6, the sensitivity and gain of the CC-202IP multi-stage RF amplifier, operating at 2.5Ghz, the 70dB gain creating a sensitivity of 280uV rms or 800uV pp, creating an output SNR of -161dBc making this configuration suitable for high gain LNA, RF amplifier, and PLL applications. As shown in Figure 4, he CC-201IP is cascaded to create any desired gain or tunable bandwidth, creating an adjustable and tunable CC-202IP block.

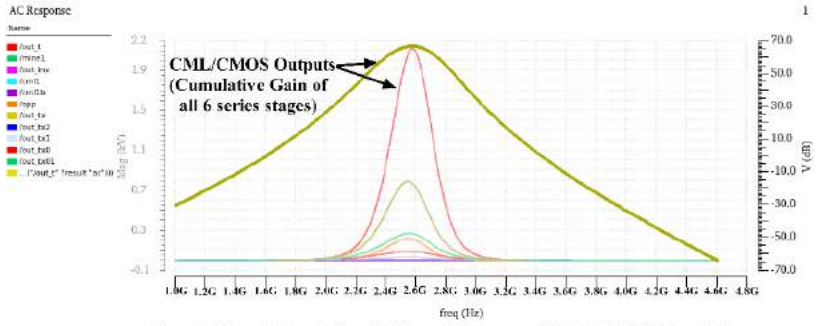


Figure 6: Cumulative Gain of 6 Cascaded Stages with CML/CMOS Level Outputs

Point of Reference for the CC-201IP and CC-202IP

As a point of reference, Figure 7 shows the phase noise of series of 3 connected CMOS inverters that would be utilized in most clock driven systems. The cumulative phase noise is 29nV rms which would yield a clock SNR of about -150dBc. This performance, when compared to the almost zero phase noise

and approaching theoretical SNR of the 2 stage gain CC-201IP CML/CMOS cell shown in Figure 3(1.3nV rms and -171dBc SNR), clearly shows the radical breakthrough that the CC-201IP, the CC-202IP, and CC-203IP designs and technology brings to systems needing substantially reduced classical noise.

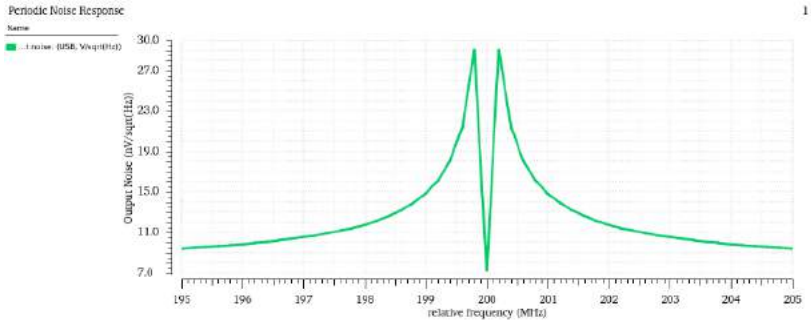
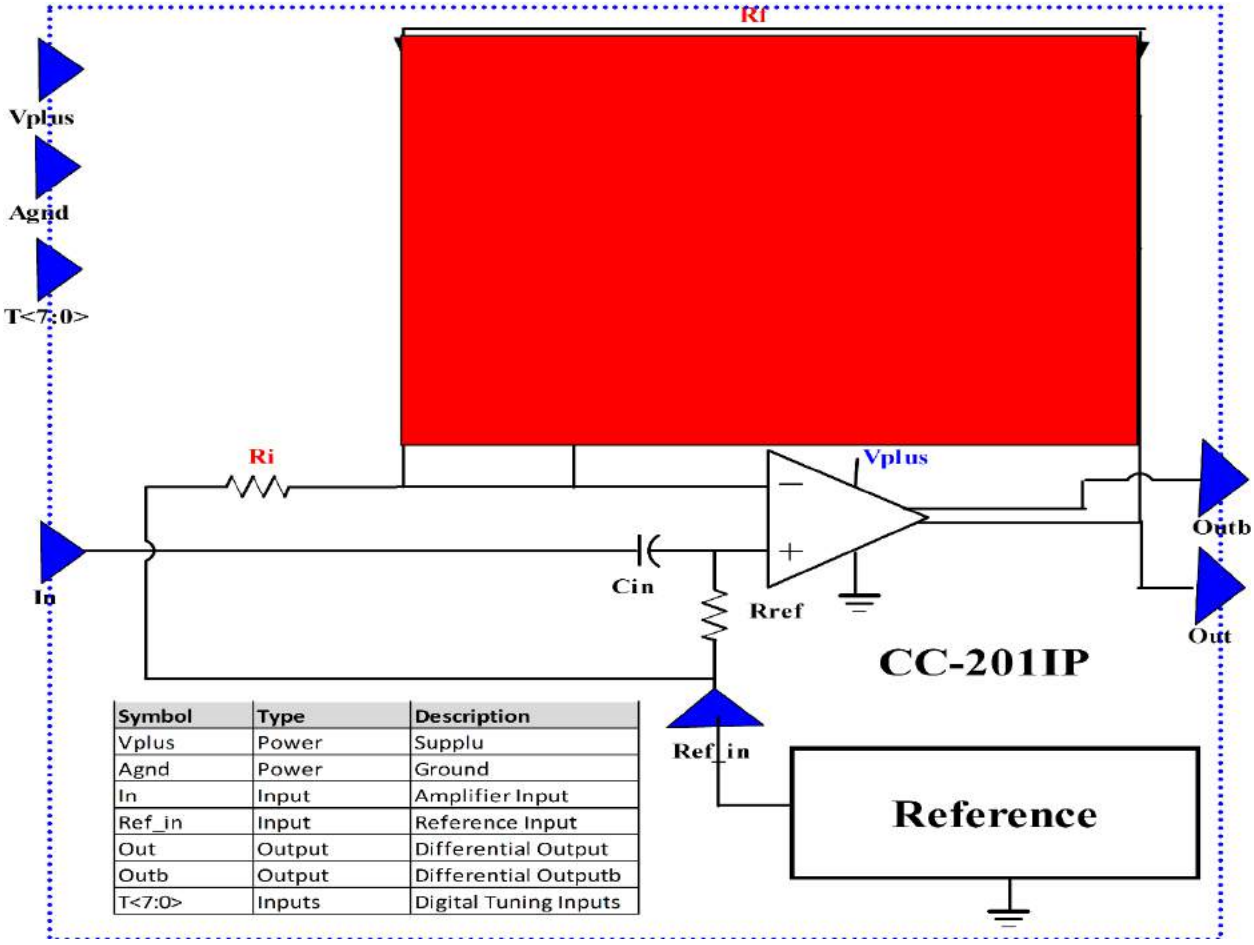


Figure 7: Typical CMOS Clock Phase Noise

Conclusion

The CC-201IP, CC-202IP and CC-203IP, greatly reducing classical noise, and the CC-100IP (see the included data and information) greatly reducing digitally generated supply line and substrate noise, both of these IP blocks utilized and working in tandem on chip, can yield a clock environment that increases sensitivity for sampled systems, and increase fidelity for Analog and RF system outputs.

CC-201IP and CC-202IP Block Diagrams, Architectures, and Pinouts



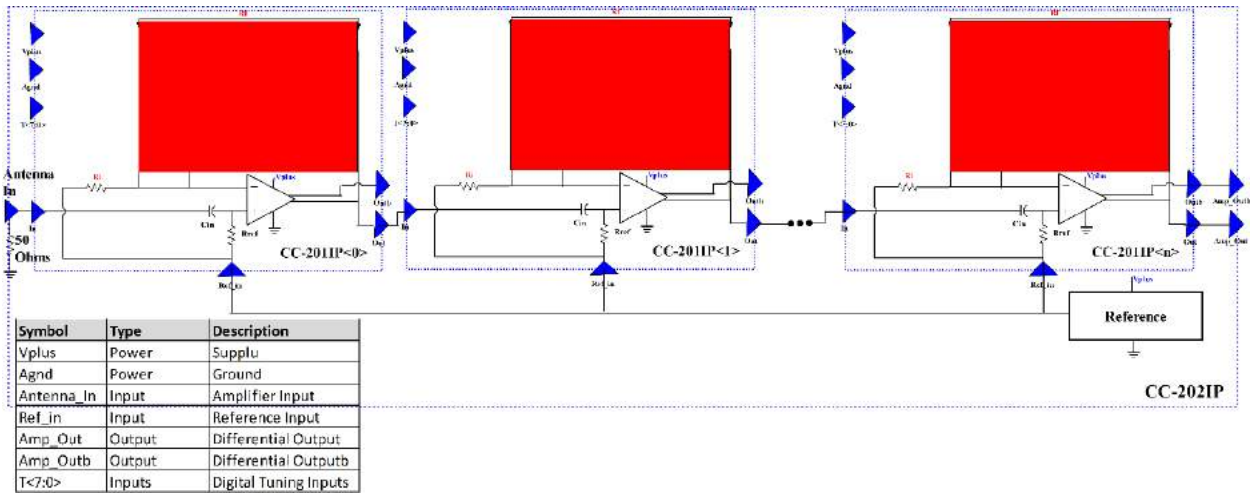
Symbol	Type	Description
Vplus	Power	Supplu
Agnd	Power	Ground
In	Input	Amplifier Input
Ref_in	Input	Reference Input
Out	Output	Differential Output
Outb	Output	Differential Outputb
T<7:0>	Inputs	Digital Tuning Inputs

Figure 8: CC-201IP Block Diagram and Pinout

Figure 8 shows the block diagram of the CC-201IP architecture. The CC-201IP is the basic IP building block of the multistage CC-202IP described above and shown in Figure 9 below. The CC-201IP Amplifier block is a basic Non-Inverting Op Amp architecture with a proprietary and patented ultra-low noise feedback component (in **RED**). The Feedback mechanism in the CC-201IP and CC-202IP is tunable (T<7:0>) for bandwidth, frequency range, and selectivity adjustment. Presently, the tuning range can be adjusted from 50Mhz to over 2.5Ghz, and can be designed to cover a broader and higher range, if desired. Contact CurrentRF for further details.

The CC-201IP and CC-202IP blocks contain their own bandgap reference for the local generation of the voltage mode Ref_In reference and biasing currents for the CC-201IP and CC-202IP blocks. The Ref_In pin can be brought out to the top level of the chip for additional bypassing.

Vplus can be any supply voltage that is compatible with the process node chosen for the CC-201IP and/or CC-202IP. Given the appropriate process node, the Vplus supply can range from 3.3V to 1V.



Symbol	Type	Description
Vplus	Power	Supplu
Agnd	Power	Ground
Antenna_In	Input	Amplifier Input
Ref_in	Input	Reference Input
Amp_Out	Output	Differential Output
Amp_Outb	Output	Differential Outputb
T<7:0>	Inputs	Digital Tuning Inputs

Figure 9: CC-202IP Block Diagram and Pinout

Figure 9 shows the block diagram of the CC-202IP architecture. The CC-202IP consists of multiple CC-201IP blocks connected in series, the T<7:0> ports tied together and "gang tuned" in order to get a higher gain and steeper bandpass function, at the expense of slightly higher classical noise (1.3nV per root Hz with the CC-201IP single cell, 8nV per root Hz with the 6 cascaded stages of the Figure 4 CC-202IP example). The ultra-low noise proprietary and patented feedback component in each of the CC-201IP cells that are used to construct the CC-202IP architecture facilitate the cascading capability of the CC-202IP due to the ultra-low noise aspect of the component. Presently, the tuning range of the CC-202IP can be adjusted from 50Mhz to over 2.5Ghz, and can be designed to cover a broader and higher range, if desired. Contact CurrentRF for further details.

The CC-202IP block contain it's own bandgap reference for the local generation of the voltage mode Ref_In reference and biasing currents for the CC-201IP and CC-202IP blocks. The Ref_In pin can be brought out to the top level of the chip for additional bypassing.

Vplus can be any supply voltage that is compatible with the process node chosen for the CC-201IP and/or CC-202IP. Given the appropriate process node, the Vplus supply can range from 3.3V to 1V.

Contact Information:

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