CC-100 IC Demonstration Platform And Applications

This document is a guide to CC-100 integration into DSP and processor based systems. It is partitioned into 2 steps. The first step is intended to be a familiarization step, using the CC-100 Demonstration Platform as a standalone demonstration, evaluation, and verification vehicle. The second step, Performance Integration into Customer Systems, is the actual integration of the CC-100 IC and circuits into a given Systems Platform, using the experience and learning gained in exercising the demonstration platform in the first step, enabling integration and evaluation success of the CC-100 in given IC systems. Contact CurrentRF for details on this process.

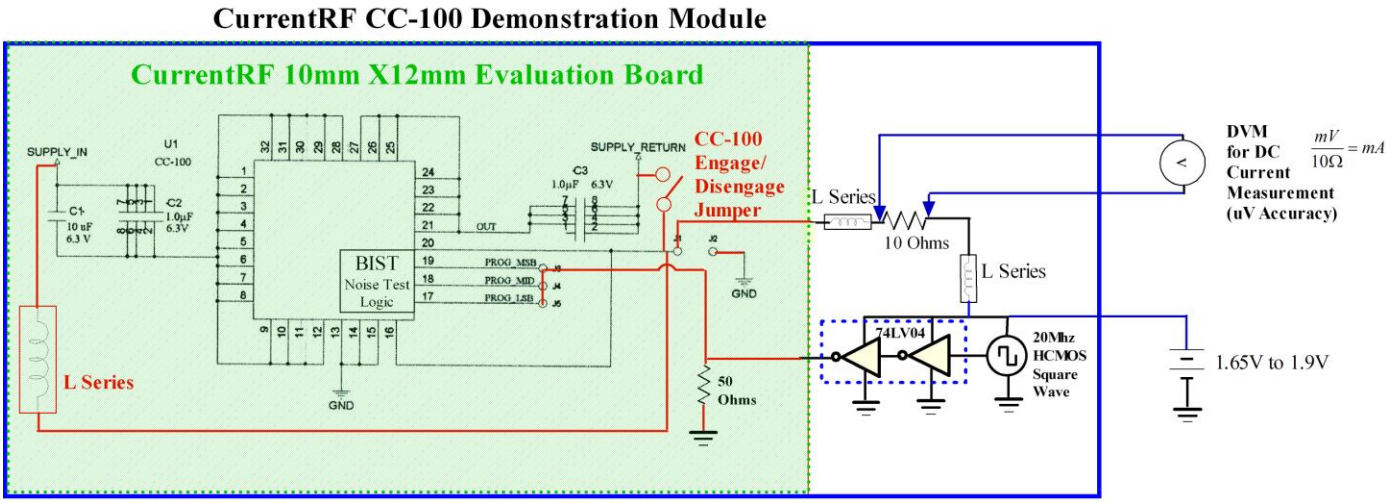
Step 1: CC-100 Demonstration, Evaluation, and Verification

Figure 1 below shows the schematic details of the CC-100 Demonstration Platform. The Platform is constructed in such a manner that one only needs the materials outside of the **blue** polygon in Figure 1. An adjustable 1.65V to 1.9V power supply, and a DVM capable of DC micro-volt resolution is all that is needed to evaluate the CC-100 on this platform. The actual lab test setup is shown in Figure 2.

The Demonstration Platform utilizes ten, .18um, 1.8V logic gates, configured as a thermometer decoder embedded in the CC-100, as circuitry utilized as a BIST Noise Test generator(see Figure 3). There are no 1.8V supply DCAPs inside the CC-100, thus high frequency noise energy is output to the C1, C2, and C3 caps on the CC-100 Evaluation Board(see Figure 4), enabling CC-100 current and power reduction operation.

Typical CC-100 performance metrics are summarized in Figure 1 and shown in Table 1, showing that the performance of the CC-100 will change with supply variation(the output slew rate of the CC-100 internal logic varies with supply voltage) and with the slew rate and duty cycle characteristics of the onboard clock generator.

The CC-100 power reduction performance is seen to vary from around 5% supply current reduction to over 24% with proper lab setup.



BIST Noise Test Logic=10 Logic gates(And, Or, Inverters)
Typical Metrics:
Supply Current- CC-100 Disengaged------> 4.249mA
Supply Current- CC-100 Engaged---------->3.774mA
Delta---------->.475mA
Percent Reduction---------->5%to 24%
Clock Rate---------->20 Mhz
Supply Voltage---------->1.65 V to 1.9V

Figure 1: CC-100 Demonstration Module and Typical Metrics

Supply Voltage (V)	CC-100 Engaged (mA)	CC-100 Disengaged (mA)	delta (mA)	Percentage Reduction
1.9	5.392	5.88	0.488	8.3
1.85	4.932	5.233	0.301	5.7
1.8	3.774	4.249	0.475	11.17
1.75	2.717	2,858	0.141	5
1.7	1.997	2.113	0.116	5.5
1.65	1.106	1.464	0.358	24.4
				(Average) 9.8

Table 1: CC-100 Demonstration Module Performance Variance with Supply Voltage

Table 1 above shows CC-100 performance over varying supply voltages (1.9V to 1.65V) with the CC-100 engaged(the black jumper installed in Figure 2) and

disengaged(the black jumper in Figure 2 de-inserted(not shown)). With the gathered raw data, the engaged/disengaged current delta and percentage current reduction with the engaged CC-100 is computed and inserted into Table 1.

The Table 1 data was gathered with a Fluke 289 True RMS Multi-meter which possesses a micro-volt precision DC DVM. A micro-volt precision DC DVM is necessary for accurate CC-100 BIST testing.

Table 1 shows somewhat high variability in the current saved by the CC-100(5% to 24%). This is not a variation in CC-100 performance, but is the result of slew rate variation in the onboard BIST generator and external clock generation circuits.

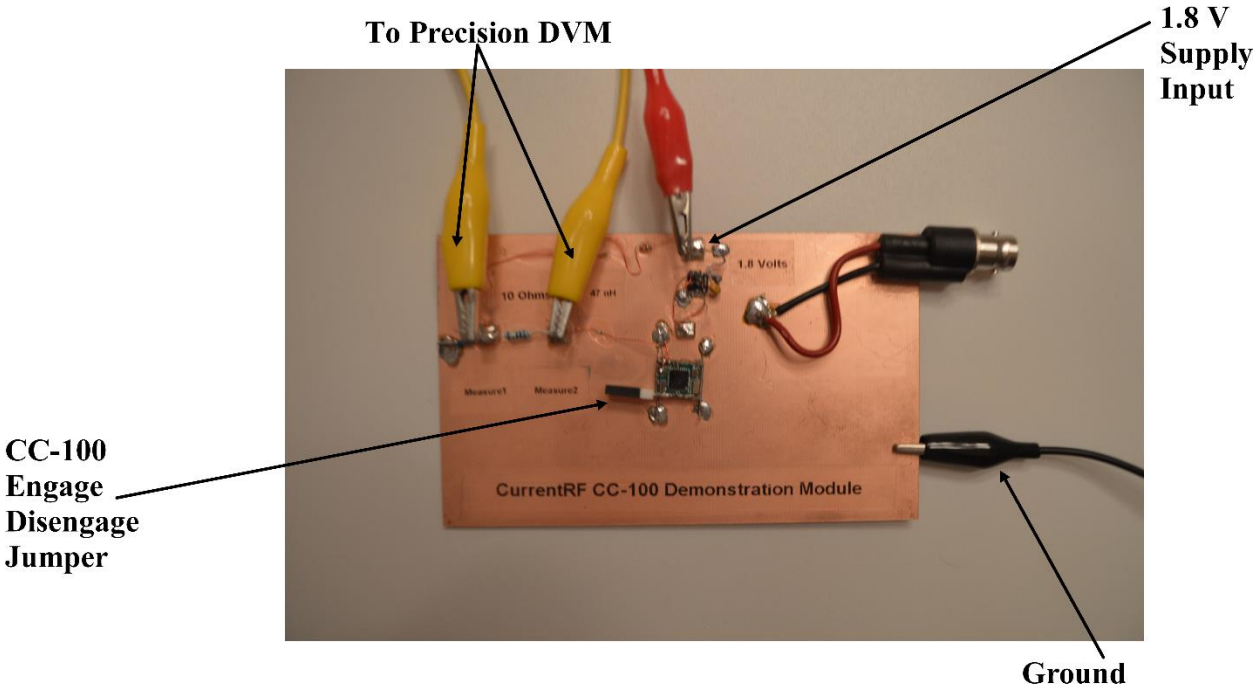


Figure 2: CC-100 Demonstration Module Lab Set-up

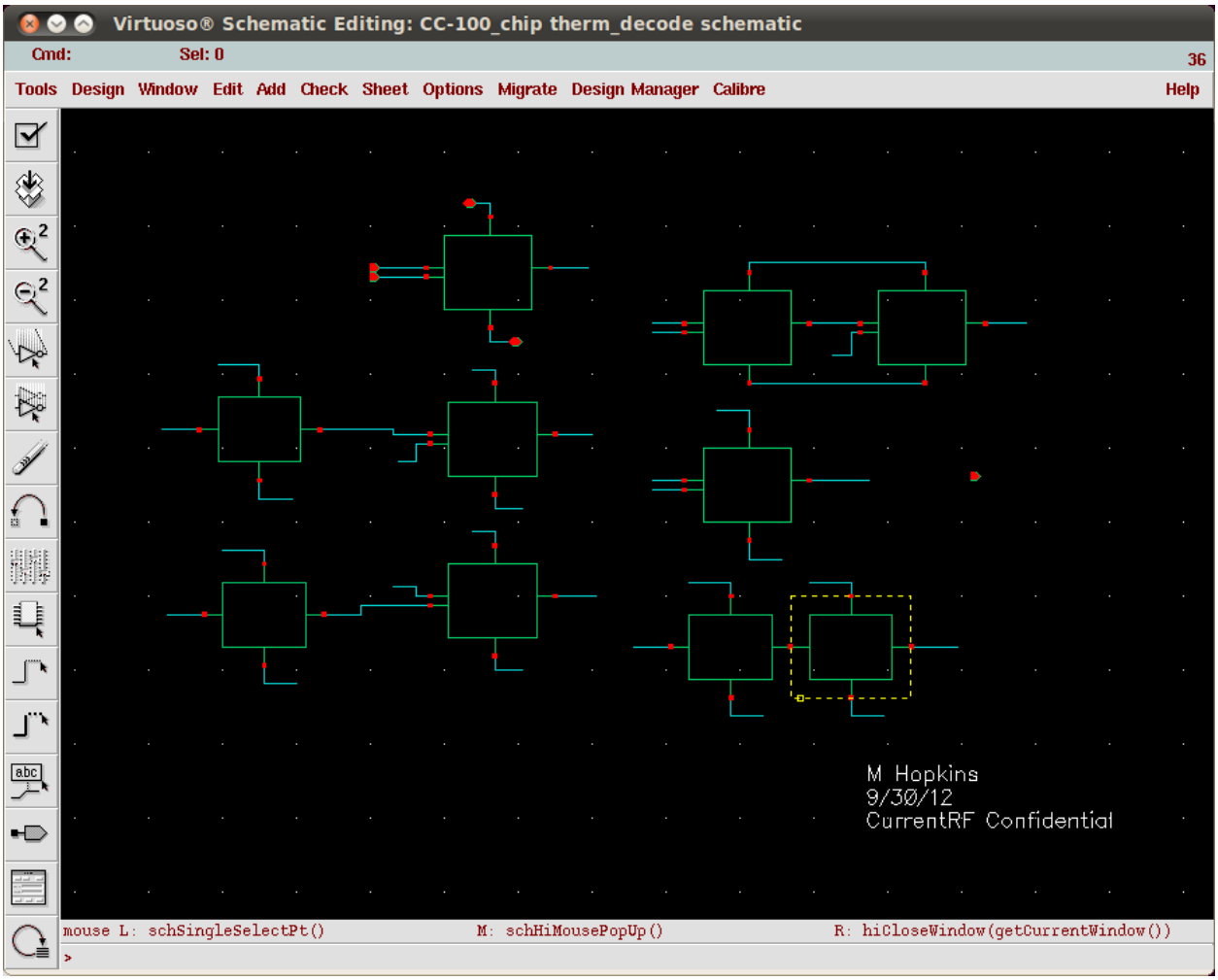


Figure 3: CC-100 Demonstration Module BIST Decoder Logic

Figure 3 above shows the CC-100 Thermometer Decoder used as a BIST Noise Engine for the CC-100 tests. Not shown are ESD cells with 250 Ohm resistor in series with the logic gate inputs and the pF range capacitances associated with the decoder inputs.

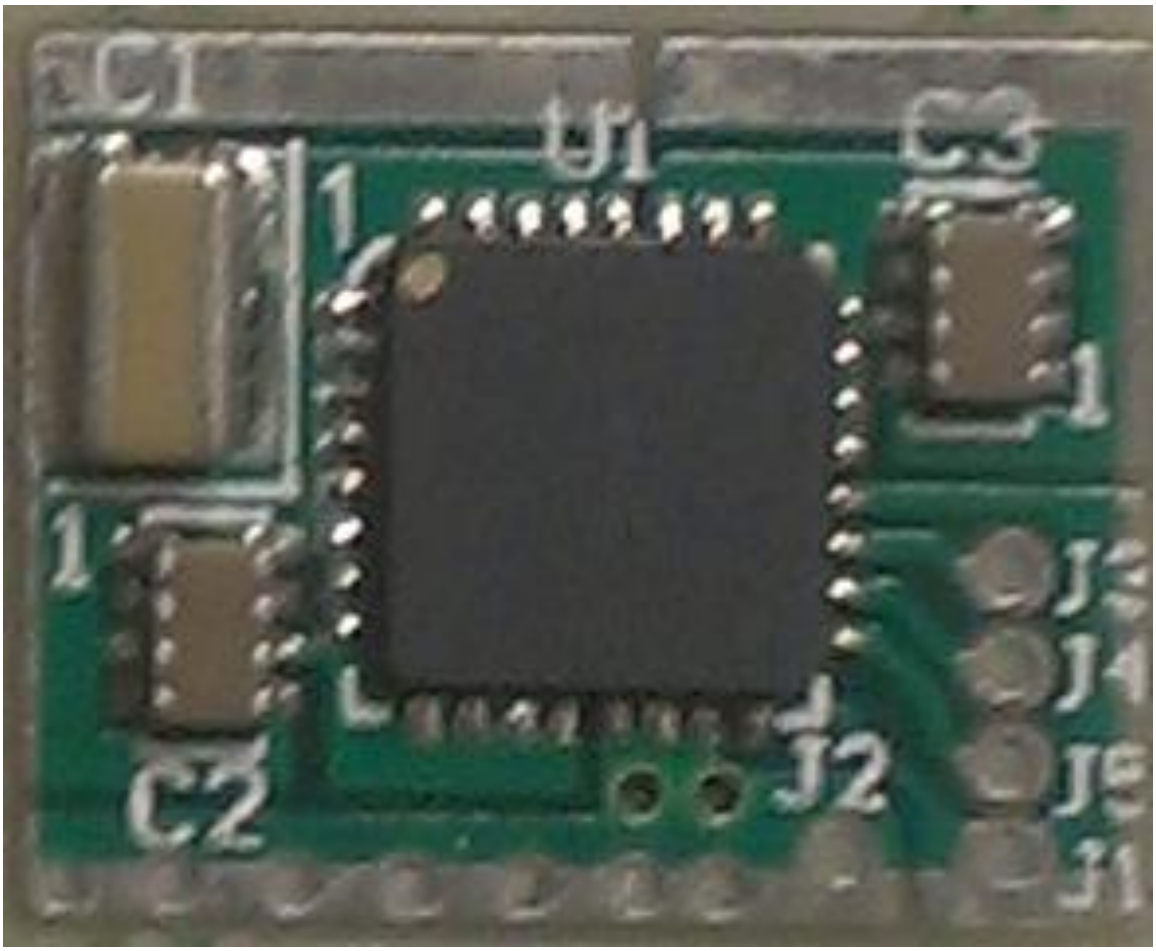


Figure 4 : CC-100 Demonstration Board

CC-100 IC Applications

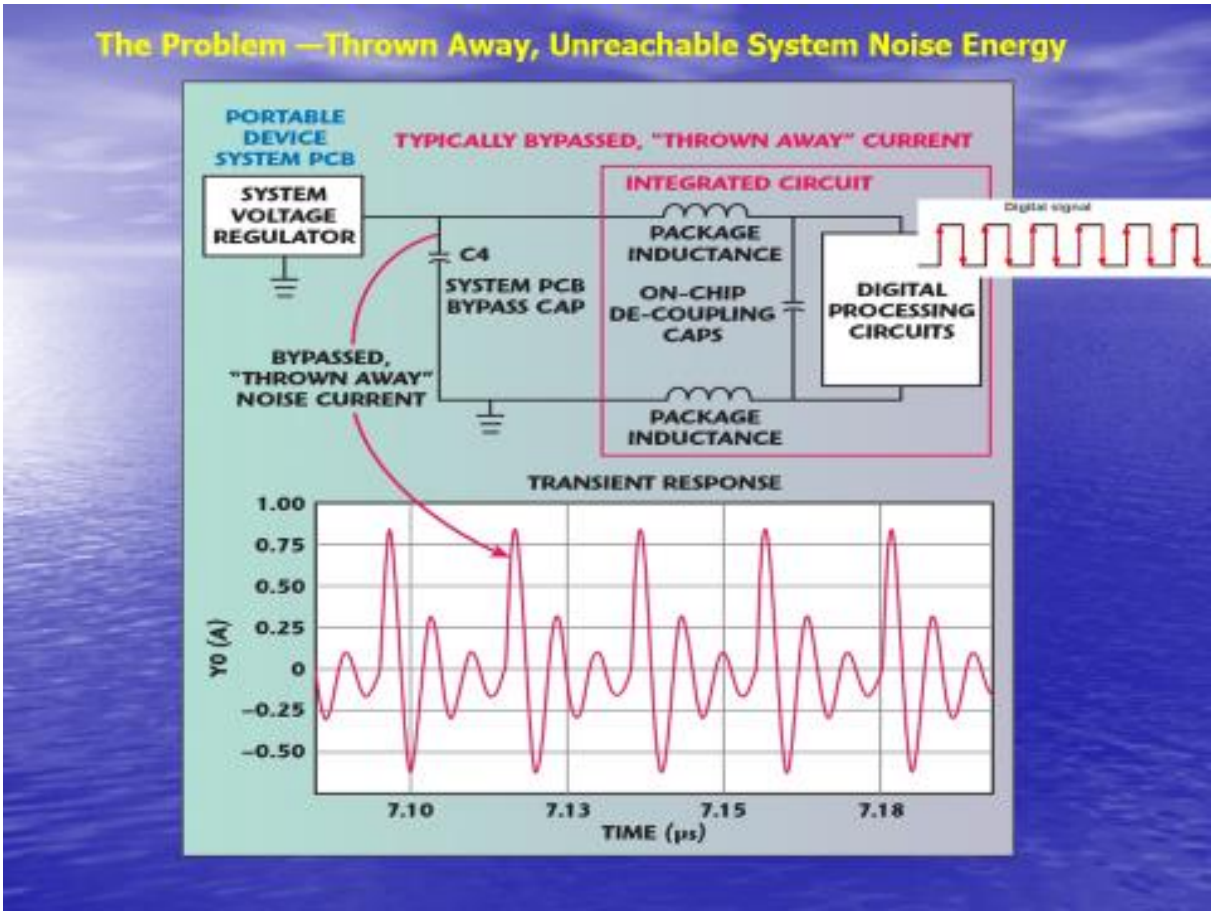


Figure 5: Typical System Power Performance

Figure 5 shows typical wasted current flowing (the "red" plot) as the result of active digital circuits and a typical system bypass cap (C4). In Figure 5, current spikes up to 1 Amp are shown. The "integrated circuit" in Figure 5 can be any IC in any system that has some amount of digital activity on board.

Power draw due to digitally derived noise currents can be greater than 50% of the total device power consumption. Digital power drain tends to increase as application complexity increases in computers and smart devices.

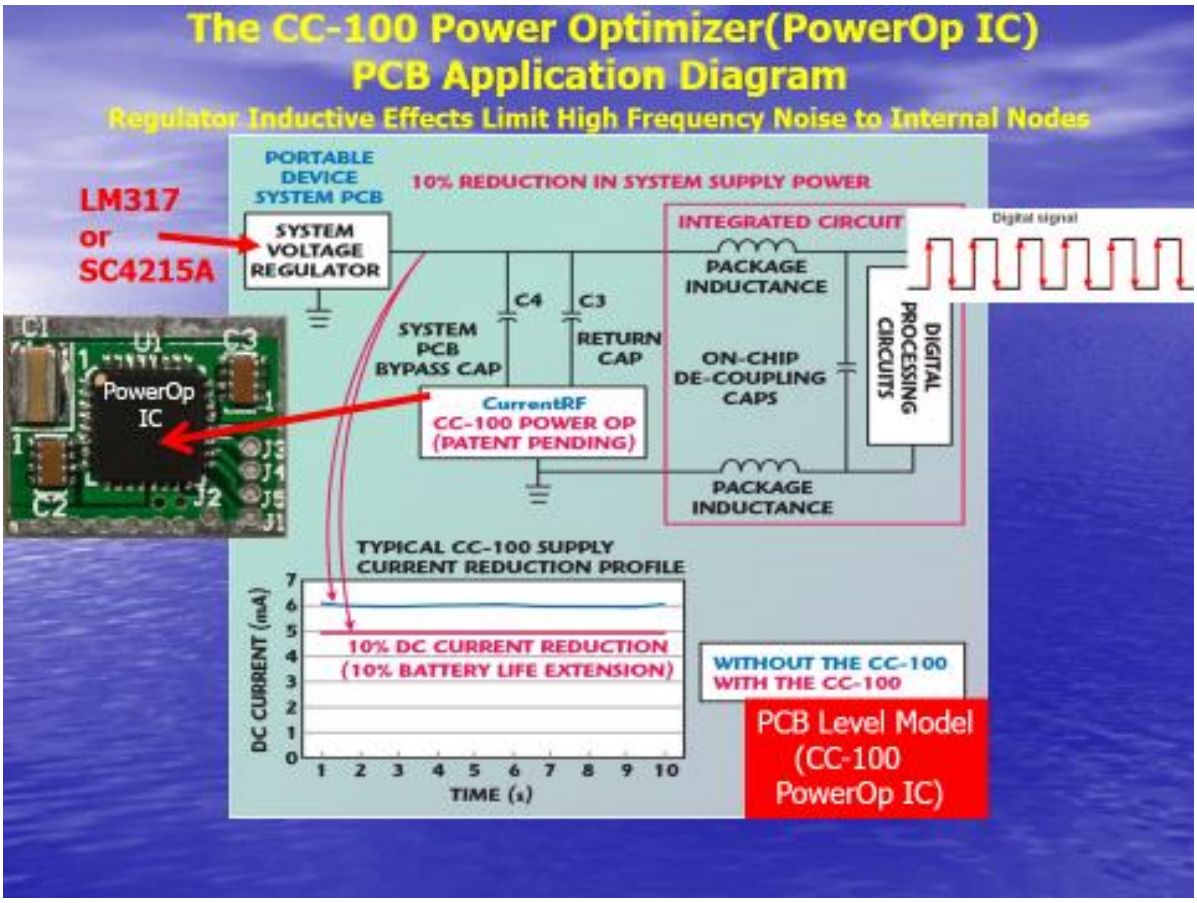


Figure 6: System Power Performance with the CC-100

Figure 6 shows the same system as in Figure 5, only this time the CC-100 is inserted in series with the ground path of the system decoupling path and a current return cap (C3) is included for the CC-100 return path. The system bypass cap (C4) is the same cap as in Figure 5.

The CurrentRF CC-100 Power OP is designed to intercept these “thrown away”, digitally generated, noise currents and recycle them back into the system. This

current recycling(the source being the 1A peak current plot in the Figure 5 case) is shown to improve system current consumption and battery life (see current draw reduction—the "red" plot in Figure 2) in the system by 10%.

Designed to be inserted in series with the ground side of a major system board bypass capacitor, the device possesses an adjustable, ultra-low input impedance small enough so as not to interfere with the normal function of a PCB bypass capacitor.

The output impedance of the CC-100 is high enough to force, with the inclusion of an appropriately sized return capacitor, "thrown away" currents back into the system.

CC-100 Evaluation Board/Reference Design

Figure 7: 10mm X12mm CC-100 Evaluation Board

The CC-100 evaluation board, shown in Figure 7 above, is designed to allow the user to easily assess "real world" power savings in any system. It is intended to be a reference design for the CC-100 IC.

The evaluation board is 2 layer board, the bottom layer(not shown), plated without solder mask, assuring the most optimal low inductance ground connection possible.

Since the board or the part requires no supply or power, the 10mm X 12mm board is designed to replace, for evaluation, any bypass capacitor in any system. The bottom layer of the CC-100 evaluation board is designed to be soldered directly to the system ground plane. For best CC-100 evaluation, it is highly suggested that the large, 1uF to 10uF capacitors, resident in all systems, be replaced by the CC-100 evaluation board for CC-100 evaluation.

On this simple board, capacitors C1 and C2 in Figure 24 function as the normal system bypass capacitors, C3 in Figure 24 functions as the CC-100 return path.

Figure 8: Low Slew Rate Operation Circuit

The CC-100 acts and recycles energy on logic transitions with high slew rate edges. The device is totally dependent on the quality, edge transition slew rate, and the speed of the logic and switching circuits from which it harvests and recycles energy.

In some cases, the CC-100 encounters logic and switching systems that possess edge transition slew rates that are lower than 5ns (the CC-100 Demo Board being one example), causing the CC-100 to operate with lower efficiency. In these cases, it is suggested that a high Q, 20nH inductor, as shown in Figure 8, be inserted in series with the CC-100 input to restore proper device efficiency. The same effect can be accomplished by driving fewer input pins on the CC-100 device, thus increasing the device and application circuit's effective input inductance.

Using Board and Plane Implementation

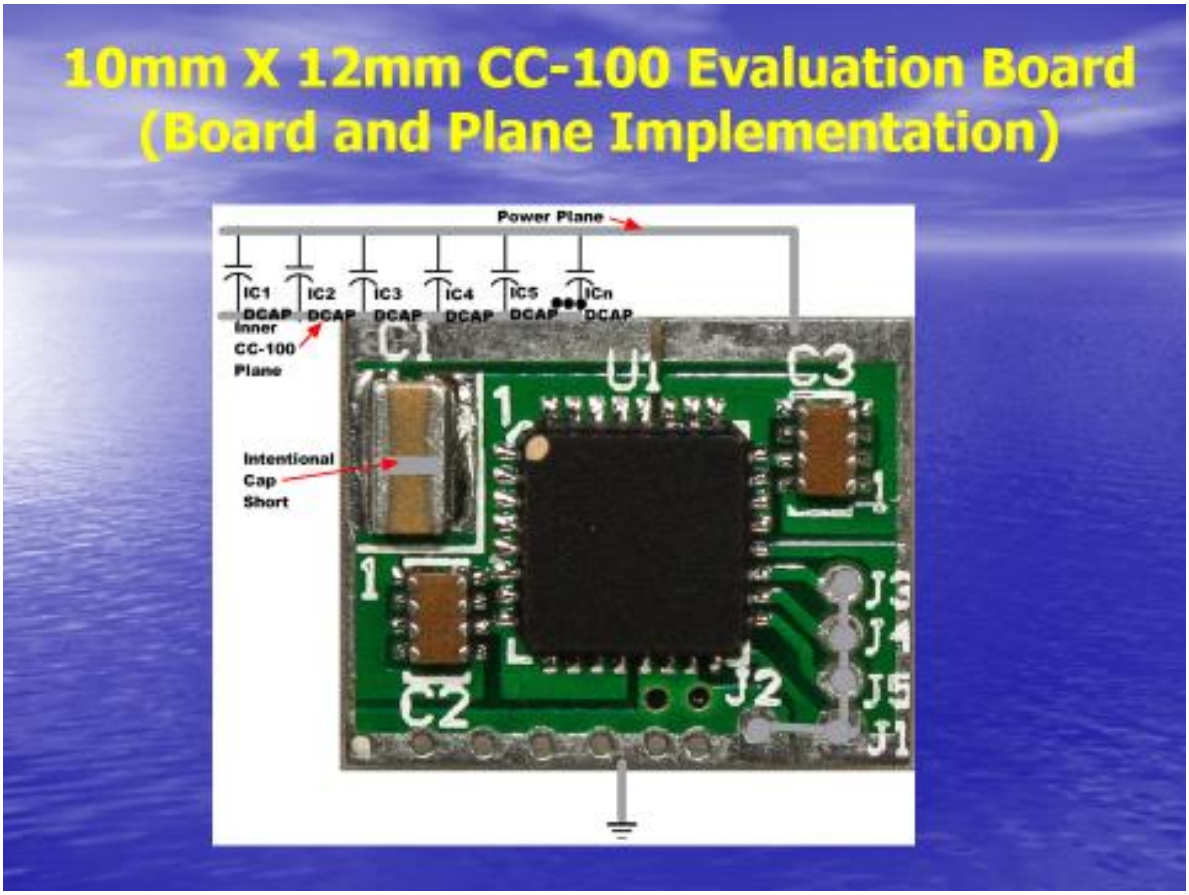


Figure 9: Board and Plane Implementation

More waste system energy may be captured and recycled by the CC-100 if all system logic bypass caps are connected to a dedicated internal CC-100 PCB plane as shown in Figure 9. The caps in figure 9 bridge the system power plane and the internal CC-100 plane, creating a board level, composite input coupling capacitor for the CC-100. To implement this application, simply short the C1 input cap on the CC-100 evaluation board and directly connect the board CC-100 internal plane to the input of the CC-100 evaluation board, as shown in Figure 9. The internal CC-100 plane needs to be wide and of extremely low inductance, so as not to present an impedance to the system board supply bypassing function. The output of the CC-100 evaluation board is connect to the system power plane, as in the applications shown in Figures 7 through 9.

Contact Information:

For additional information, evaluation boards/reference designs, product pricing or technical help, reach us at:

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