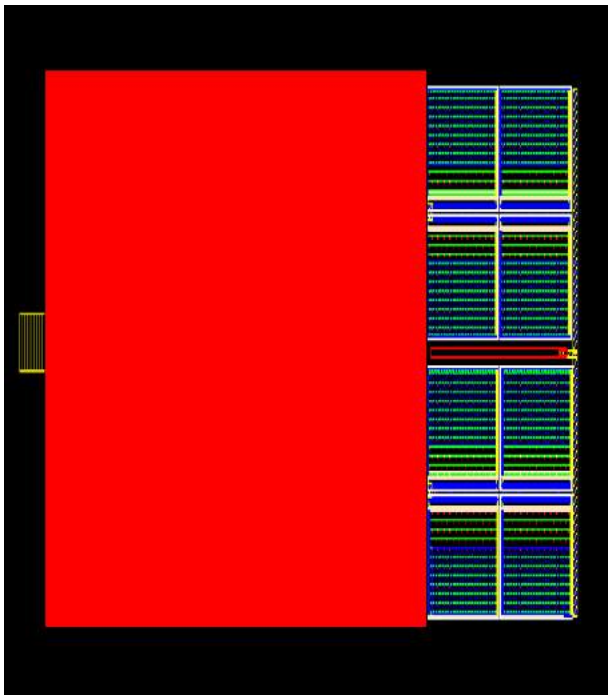
Current RF



CC-100IP-MB-Electric Vehicle Mileage Booster IP

Up to a 36% increase in EV Driving Range
Up to 2X DC-Link Capacitance Increase
25% Effective Series Inductance Reduction
Works as a Standalone DC-Link Capacitors
Works in Parallel with DC-Link Capacitors
Customized-On-Demand IP (Quick Turn Around)

General Description

The CC-100IP-MB is a noise and surge current recycling IP that resides in series with the ground terminal of Electric Vehicle DC-link and Reservoir Capacitors and system ground. The CC-100IP-MB re-cycles system noise and surge current, preventing the deep discharge of system DC-Link and Reservoir Capacitors, thus reducing the amount of deep re-charge required from EV conversion system batteries. The IP creates inherent DC-Link Capacitance Multiplication, Series Inductance Nullification, and Energy Harvesting functions that act to create the lowest Impedance point in the Conversion System Power Grids, enabling High frequency noise to be drawn into the CC-100IP-MB, aiding in maximum current recovery and Electric Vehicle Mileage extension. The IP features a circuit noise activated dynamic input current controlled reservoir capacitance, and can function as a “stand-alone” system DC-Link or Reservoir Capacitor, or work in parallel with existing DC-Link Capacitor structures. Due to the embedded IP negative feedback, the CC-100 features a 25% reduction in capacitor effective series inductance (ESL). The IP operates by feeding back a portion (nominally 20%) of the bypass current flowing through the front end on chip input base capacitors, feeding back current into the Conversion System Power Grid, preventing bypass Capacitor Deep discharge, thus reducing overall Electric Vehicle dynamic power draw.

The Mileage Booster IP is meant to replace or work in parallel with existing DC-Link and Reservoir Capacitors, thus can be shaped into various aspect ratios and sizes to fit on-chip “white space”, the area under power grids, etc. in the same fashion as typical on-chip decoupling capacitors.

Topology

Ultra-Low Impedance Input Design
Single High Impedance Output
Bi-Directional Bypass Operation
Proprietary/Patented Topology

Features

On-Chip EV Mileage Enhancement
Dynamic Reservoir Cap Power Reduction
2X Increase in DC-Link Capacitance
25% Reduction in EV System ESL

Functional Description

The CC-100IP-MB is a noise and surge current feedback block which is activated by dynamic noise current applied to it's Cap_in terminal. The embedded feedback creates conditions in which capacitive filtering is enhanced, normally thrown away current is re-cycled, and ESL is reduced, thus creating the lowest impedance point for noise in Electric Vehicle Conversion Systems. This action enhances the power reduction provided by the CC-100IP-MB.

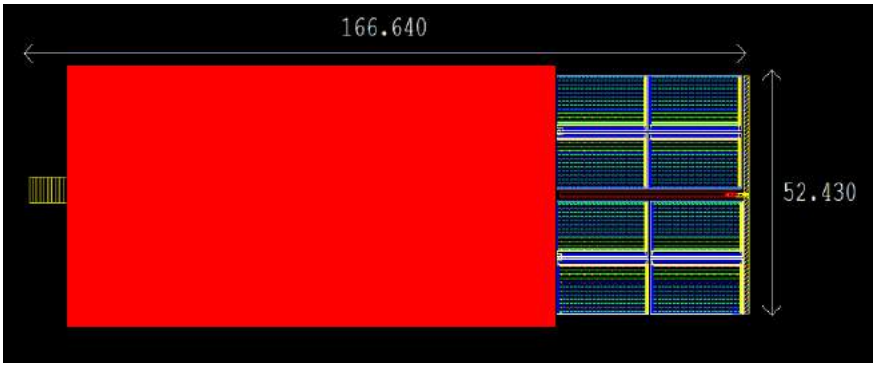
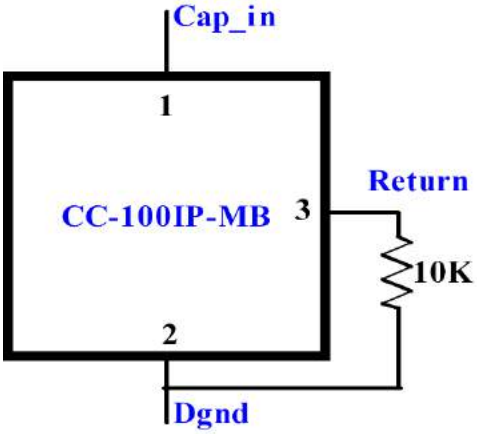


Figure 1: Typical CC-100IP-MB Aspect Ratio

Figure 1 shows the typical footprint of the CC-100IP-MB. Figure 1 shows a 166um X 53um rectangular aspect ratio footprint. The IP block can be configured into almost any aspect ratio, giving it maximum versatility and flexibility in customer designs.

The IP is designed to be placed into the "white space" on chips and under supply line power busses, in the same manner as typical on-chip DCAPs are utilized.



Symbol	Pin	Type	Description
Cap_in	1	Current	Current_input
Dgnd	2	Power	Ground
Return	3	Signal	Output Bias
			(Connect to 10K
			on-Chip Resistor)

Figure 2: CC-100IP-MB Block Diagram and Pinout

Figure 2 shows the CC-100IP-MB cell and pinout. Three connections are all that is needed for IP block operation. Cap_in is a current input from the negative side of the series DC-Link Capacitor and Dgnd is system ground. The return pin is connected to a 10K ohm on-chip bias resistor, the opposite end of the resistor connected to Dgnd.

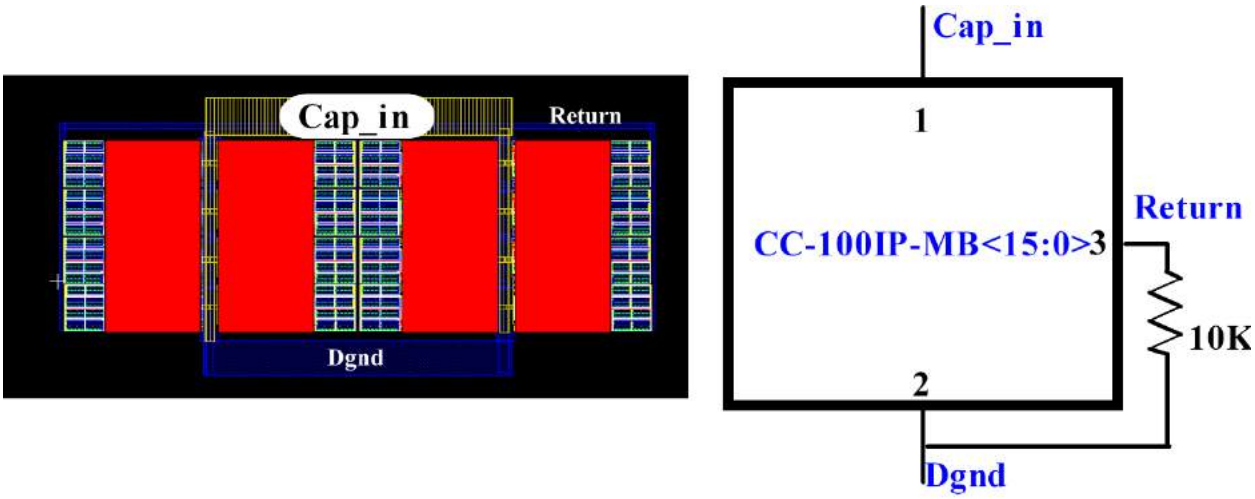


Figure 3: CC-100IP-MB Arrayed Cell Example and Block Diagram

Figure 3 shows how CC-100IP-MB IP cells can be connected in an arrayed grid pattern, forming a large, high current feedback block. In this example, sixteen CC-100IP-MB cells are connected in parallel forming a composite, large high current capability current feedback cell.

Connecting the IP is this fashion does not degrade the benefits gained from the single IP block of Figures 1 and 2 (benefits shown in Table 1). Connecting the IP blocks in parallel, as in Figure 3, the IP benefits are preserved, with the added benefits of reservoir, effective, and static capacity increases. A single on chip 10K resistor is all that is needed for biasing all the CC-100IP-MB blocks in the 16 block array and is scalable for any CC-100IP-MB array of any size.

IP/Cap Comparision Table	CC-100IP-MB Static Performance	CC-100IP-MB Dynamic Performance	CC-100IP-MB Performance Enhancement
Effective Series Inductance	100ph	75ph	25% ESL reduction vs standard DCAPs
DC-Link Capacitance	1000uF	2000uF	2X Increase in Effective DC-Link Capacitance
Actual Capacitance Scaling	1X	1x	No Change in Actual Dimensions
IP Dimensions (square um)	45	45	No Change in Actual Dimensions

Table 1: CC-100IP-MB Static/Small Signal, Dynamic Performance

Table 1 shows the static characteristics of the CC-100IP-MB and it's effects on Electric Vehicle Power Grid filtering. Given the aspect ratio of the CC-100IP-MB shown in Figure 1 (45 square microns--the approximate area underneath the red block in Figure 1) the Effective Series Inductance (ESR) is 100pH. When the CC-100IP-MB is dynamically activated, the ESR of the IP drops by 25%, to 75pH in this example. The DC-Link Capacitance increase is not actual static Capacitance increase but an effective DC-Link Capacitance increase due to the negative feedback effect on existing DC-Link Capacitance in the EV systems. The reduction in system ripple magnitude (see Figures 6 through 9) due to the CC-100IP-MB current mode negative feedback activity reduces the ripple by a factor of 2, as if doubling the DC-Link Capacitance, without the penalty of additional Dynamic current draw. In fact, the CC-100IP-MB actually saves up to 36% in

dynamic current draw from system batteries, thus increasing filtering by a factor of 2, while reducing power draw by up to 36%.

Electric Vehicle Applications

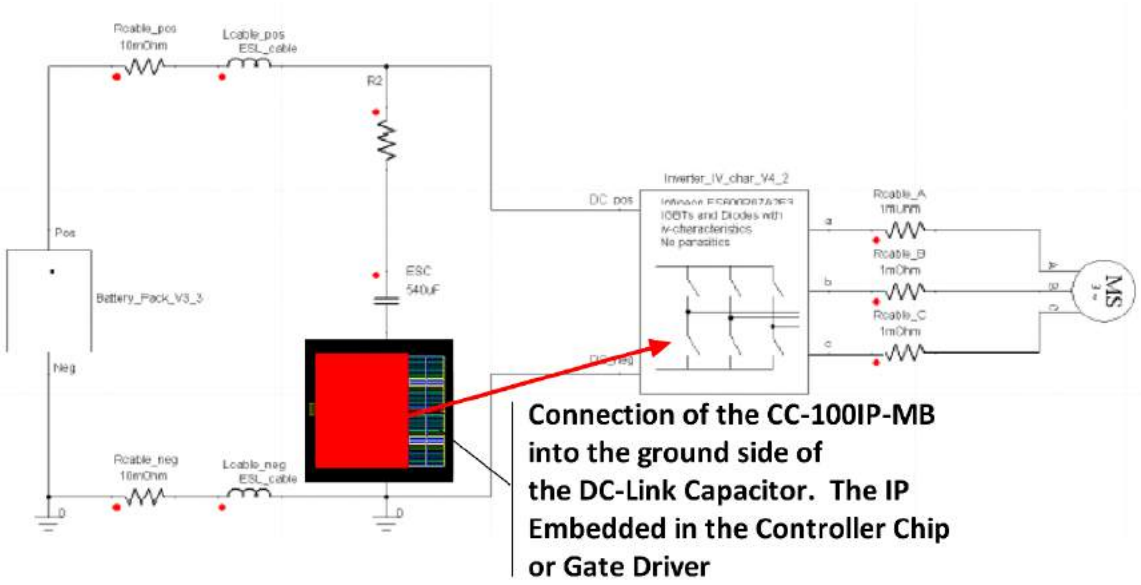


Figure 4: Schematic for the CC-100IP-MB Controller/Traction Inverter Application

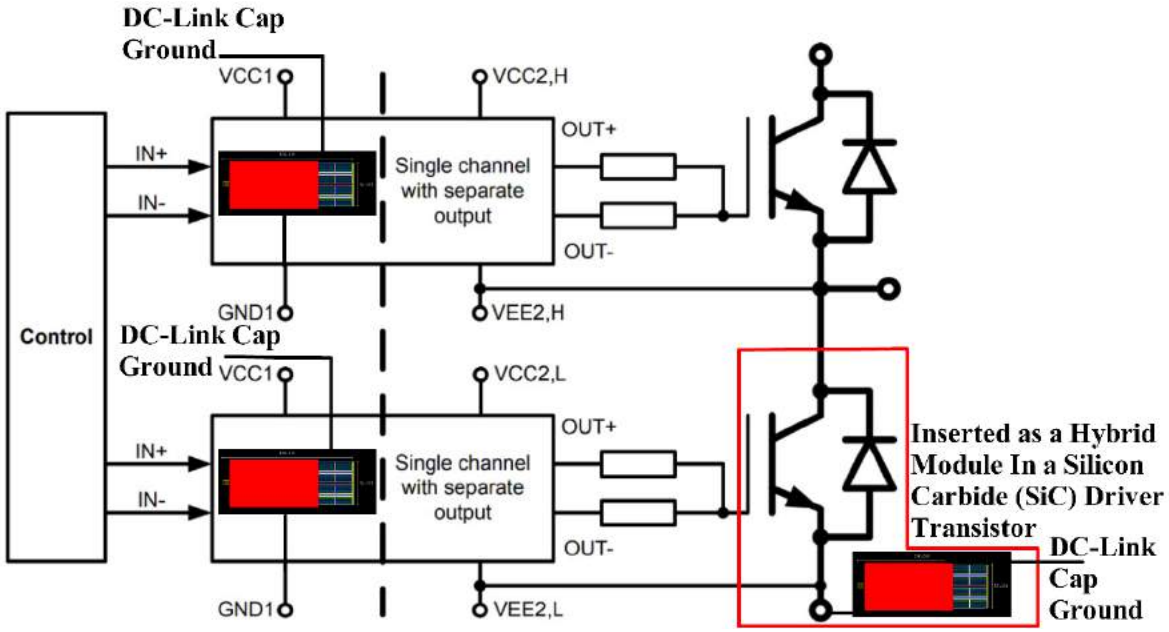


Figure 5: Traction Inverter Gate Driver and Driver CC-100IP-MB IP insertion

Figures 4 and 5 show the Electric Vehicle applications for the CC-100IP-MB IP. Figure 4 shows the general location of the IP in Electric Vehicle systems, connecting to the ground side of DC-Link and Reservoir Capacitors and system ground. Figure 5 gives

more specifics on where the CC-100IP-MB IP can be inserted, in one case the low voltage side of Traction Inverter Gate Driver ICs, and secondly, as a hybrid addition to Silicon Carbide (SIC) Driver Transistors,

In any case, the CC-100IP-MB IP is scalable on chip, with more parallel connected unit cells, to adjust for maximum current capability required in the system.

Time Domain/Mileage Extension Performance

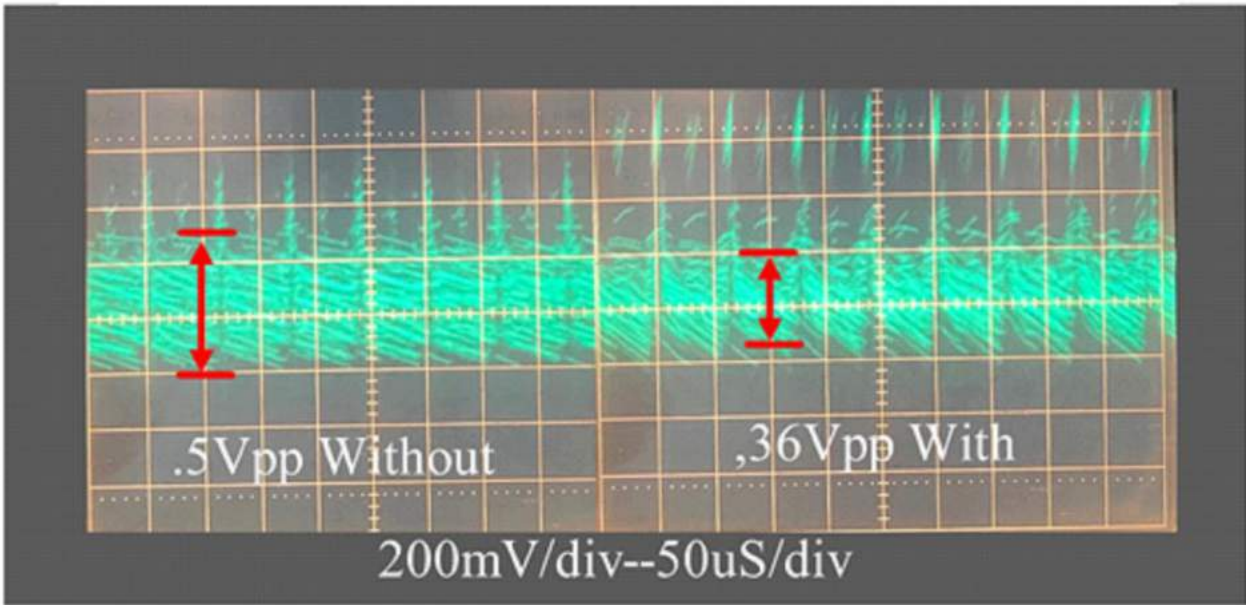


Figure 6: CC-100IP-MB E-Bike Disengaged/Engaged Time Domain Performance

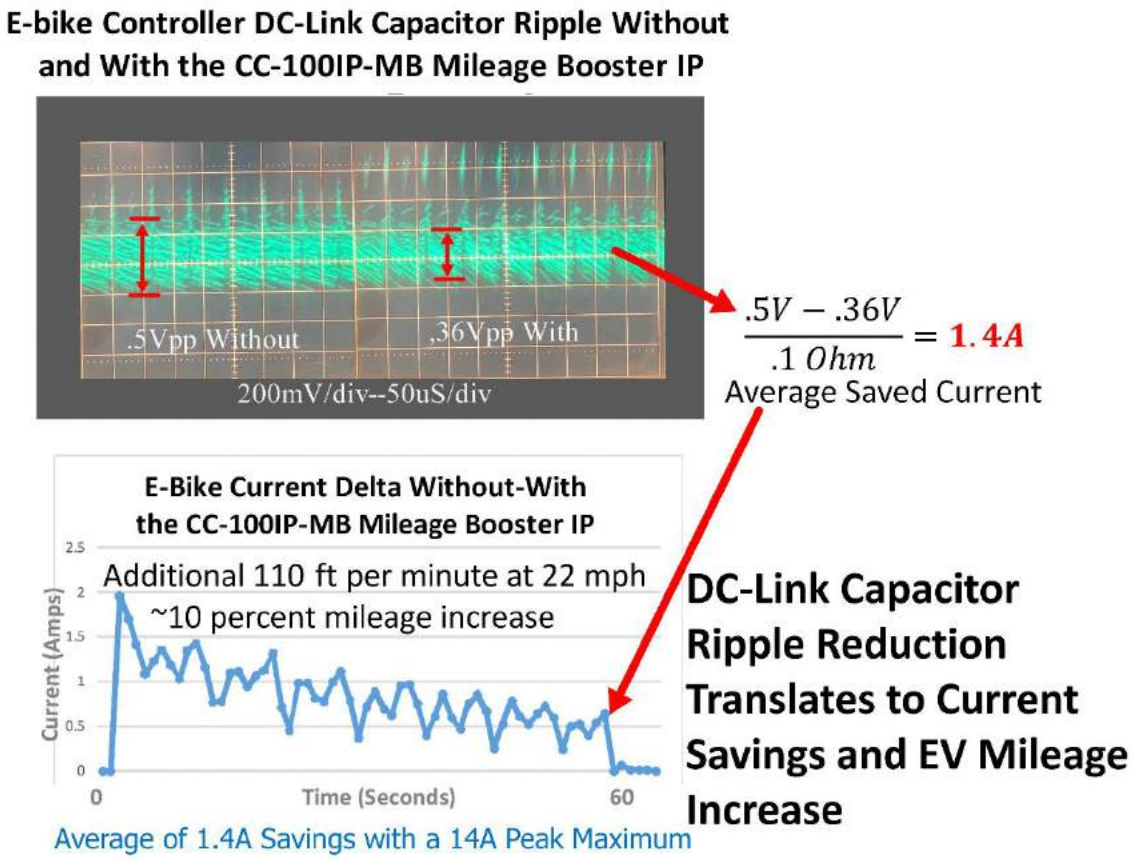


Figure 7: E-Bike Current Savings and Mileage Increase Analysis

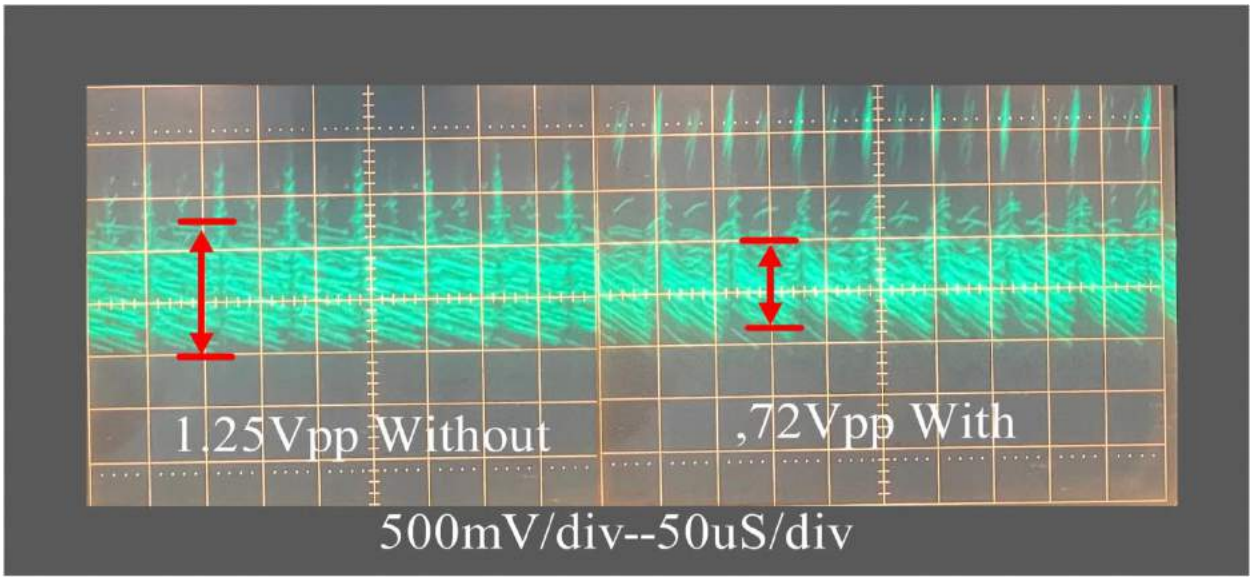


Figure 8: CC-100IP-MB EV Traction Inverter Disengaged/Engaged Time Domain Performance

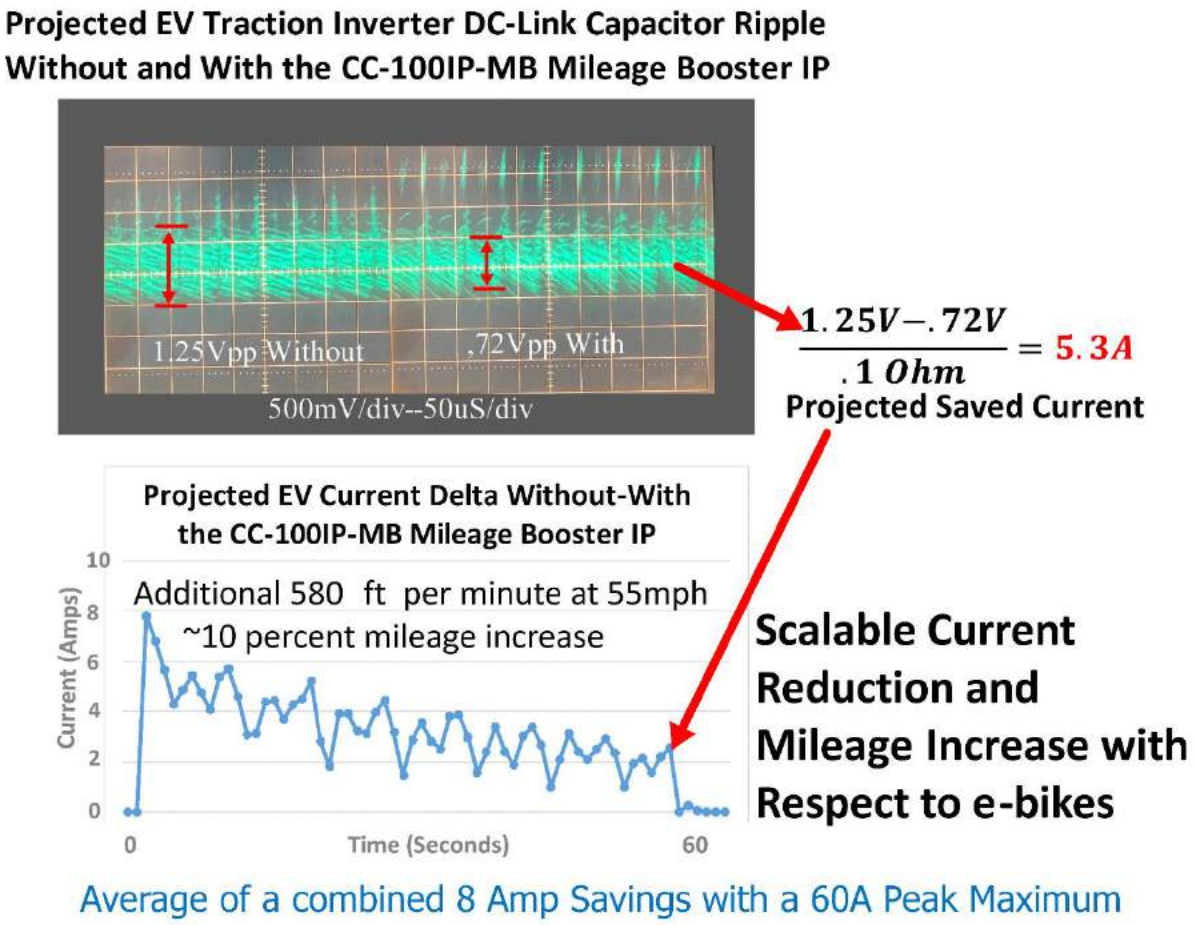


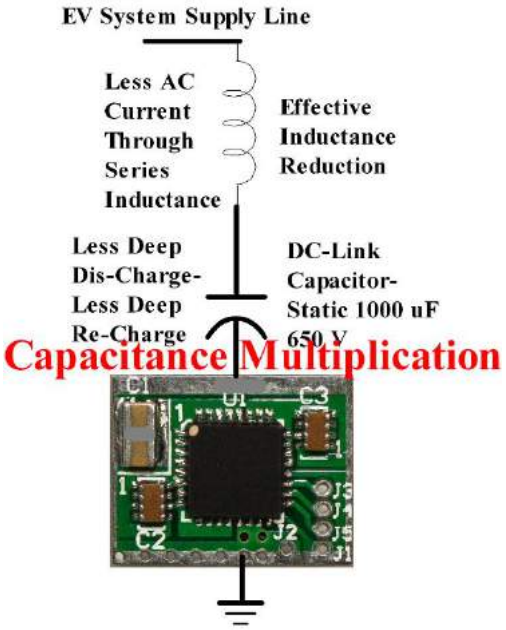
Figure 9: EV Projected Current Savings and Mileage Increase Analysis

Figures 6 through 9 show the DC-Link and Reservoir Capacitor ripple reduction and how it relates to CC-100IP-MB current savings and consequent Electric Vehicle Mileage increases.

Figures 6 and 7 show the performance results of dis-engaging and engaging the CC-100IP-MB IP when applied to E-bike controllers, Effectively, the CC-100IP-MB IP saves 1.4A of current during e-bike operation, which translates to an additional 110ft per minute during the e-bike ride. Given 13 hours of e-bike ride time, the additional mileage accumulated with the CC-100IP-MB IP equals over 16 miles of additional e-bike riding range.

Figures 8 and 9 show the performance results of dis-engaging and engaging the CC-100IP-MB IP when applied to Traction Inverter Systems, In Electric Vehicle Systems, everything scales and the CC-100IP-MB IP saves 5.3A of current during Electric Vehicle operation, which translates to and additional 580ft per minute during the Electric Vehicle drive at 55 mph. Given 4.5 hours of Electric Vehicle Drive time, the additional mileage accumulated with the CC-100IP-MB IP equals over 30 miles of Electric Vehicle Driving Range.

Static/Dynamic Characteristics



Small Signal Broadband Impedance-- Broadband Frequency Response-System Lowest Impedance Point

Silicon Proven CC-100 Test Chip IP, shown to the right, of which the CC-100IP-MB is a base component, Figures 10 through 16 show the results of CC-100IP-MB CMOS7RF (Global Foundries) AC characterization. The Inductance Nullification and Capacitance Multiplication of the IP block creates the lowest impedance point in a given system.

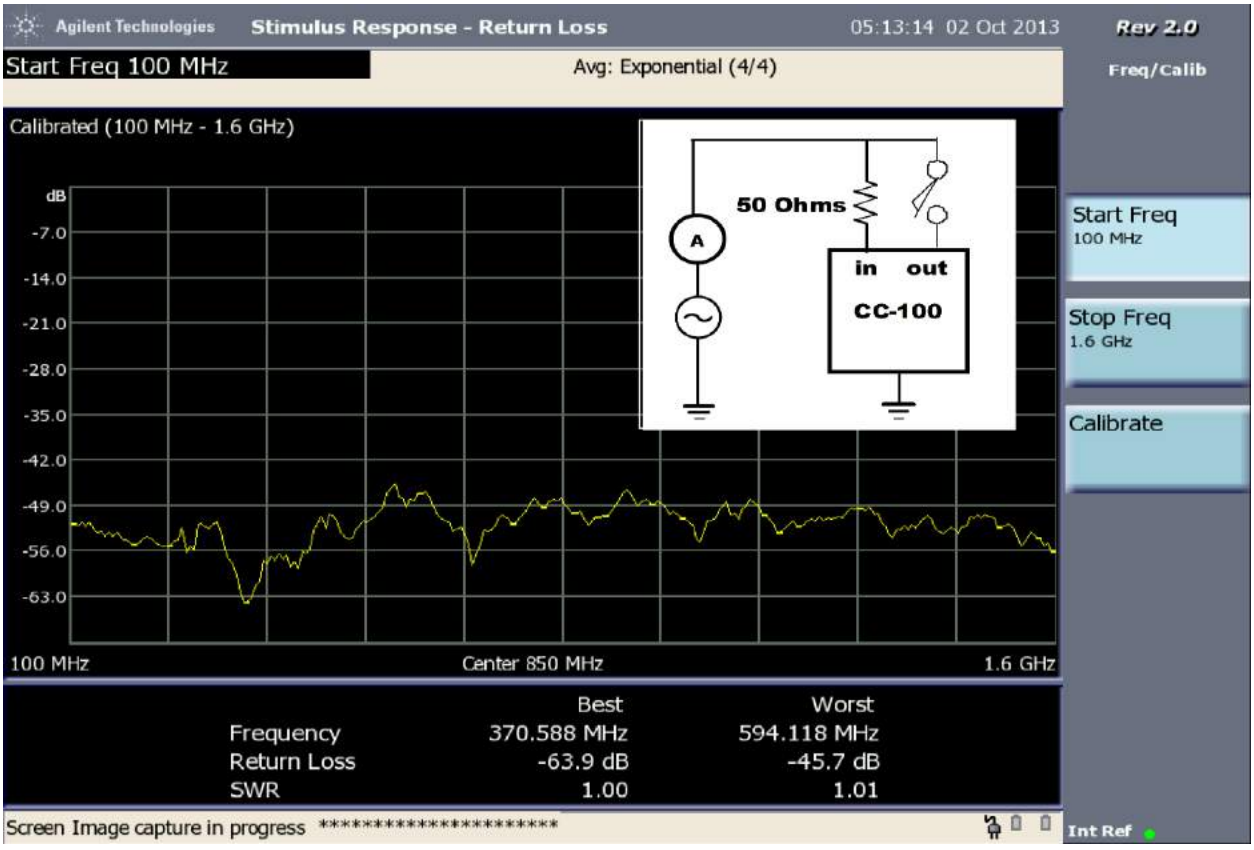


Figure 10: CC-100IP-MB Small Signal S11 Input Plot (CC-100IP-MB Disengaged)

The S_{11} return loss plot in Figure 10 graphically displays the bandwidth, input impedance, EMI suppression, and spectral response of the CC-100IP-MB Mileage Booster IP. The plot in Figure 10 shows a CC-100IP-MB bandwidth ranging from 100Mhz to 1.6Ghz and the wideband S_{11} return loss of the device. With a series 50 Ω resistor placed at the input of the device, as seen in Figure 10, the overall VSWR of the device input is quite good, varying from nearly perfect, VSWR of 1.0 at 370Mhz, to a worst case VSWR of 1.01. The Figure 10 plot shows that the low input impedance of the device is negligible to the total input resistance, and does not show much variation over the input bandwidth of the IP.

In Figure 10, with the CC-100IP-MB disengaged, looking exclusively into the 11uF input base capacitance in this example, the best return loss/SWR and the lowest impedance point occurs at 370Mhz (-64dB) and corresponds to a capacitive low impedance magnitude of 39 Micro Ohms. A short math proof is as follows.

Equation 1:

$$50 * invlog\left(-\frac{dB}{10}\right) \cong 1/(2 * \pi * f * C)$$

Using the CC-100IP-MB IP data, the lowest impedance point frequency in the Figure 10 plot, as well as the "Best" return loss and SWR numbers from the Network Analyzer, gives

$$50 * invlog(-\frac{63.9dB}{10}) \cong 1/(2 * \pi * 370Mhz * 11uF)$$

Solving yields

$$20\mu\Omega \cong 39\mu\Omega$$

Which, within measurement and error tolerances, the results are essentially equal.

Narrowband spectral peaks and dips remain, however, in Figure 10, indicative of imperfections in the matching of the power grid on the IP evaluation board, test system cabling, and connectors.

The plot in Figure 11 shows the S_{11} spectral results of the CC-100 IP's negative feedback and Electric Vehicle power grid compensation. The Figure 11 plot demonstrates an increase in overall "returned" current (a 7 dB decrease in return loss, a slightly higher worst case VSWR of 1.03 vs. 1.01), but much reduced spectral peaks and dips, with respect to the plot in Figure 10. This return loss and VSWR decrease is not due to typical load mismatch effects, but is the result of CC-100IP-MB action, returning current to the system for reuse. Thus, in the plot in Figure 11, the network analyzer power detectors show the device current return and negative feedback compensating for the imperfections present in the power grid on the CC-100IP-MB evaluation board, test system cabling, connectors, etc.

Using the same example base input capacitance, 11uF, as in the Figure 10 plot, and engaging the CC-100IP-MB IP, the best return loss/SWR the transfer function lowest impedance point is translated down to 170Mhz(-56.3dB), as seen in Figure 11. Accounting for a +7 dBm scaling with respect to the Figure 10 plot, this due to return currents flowing from the CC-100IP-MB IP output into the Network Analyzer detectors, the low impedance point corresponds to a

capacitive low impedance of 42 Micro Ohms. This low impedance dip in Figure 11 fits the impedance and frequency characteristic that would be seen utilizing a standard 22uF capacitance. This measurement confirms the effective capacitance increase generated by the action of the Silicon Super Capacitance IP. The math for this condition as follows.

Equation 2:

$$50 * invlog((-dB - 7dB)/10) \cong 1/(2 * \pi * f * C)$$

Using the CC-100IP-MB IP data, the lowest impedance point frequency in the Figure 11 plot, as well as the "Best" return loss and SWR numbers from the Network Analyzer gives

$$\left(50 * invlog\left(\frac{(-56.3dB-7dB)}{10}\right)\right) \cong 1/(2 * \pi * 170Mhz * 22uF)$$

Solving yields

$$23.4\mu\Omega \cong 42\mu\Omega$$

Which, within measurement and error tolerances, the results are essentially equal.

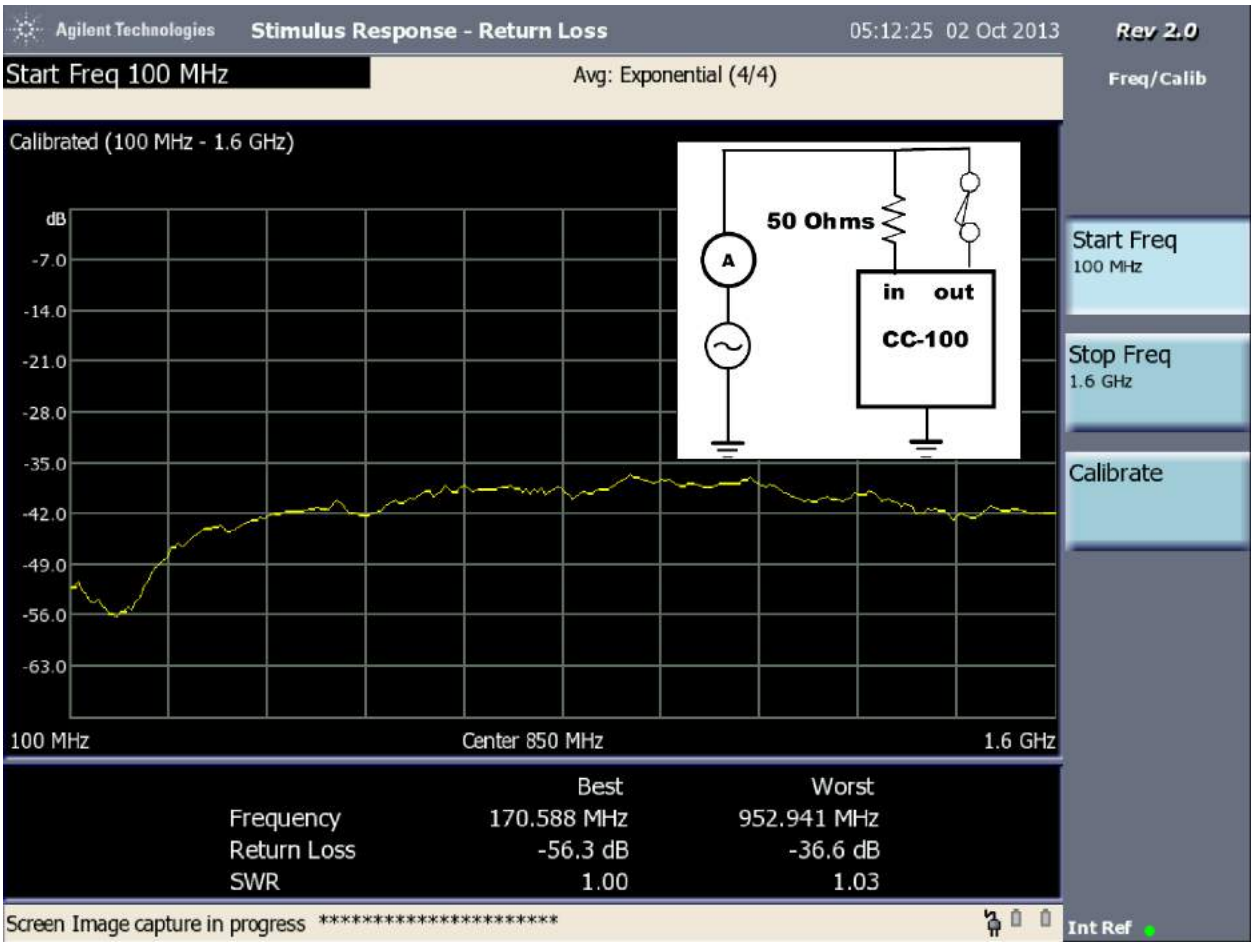


Figure 11: CC-100 IP-MB Small Signal S11 Plot (CC-100IP-MB Engaged)

Large Signal Reservoir Capacitance Behavior

In the presence of curicut noise, CC-100IP-MB forces the Input DC-Link or Reservoir Capacitance to increase up to 600X it's static Capacitance Value, this increase tracking the input noise magnitude. As the dynamic current applied through the DC-Link or Reservoir Capacitance, the Reservoir or DC-Link capacitance dynamically increases proportionally. With no dynamic current applied, the DC-Link or Reservoir Capacitance attached to the 45 square micron CC-100IP-MB shown in the Figure 1 block performs at it's nominal value. When dynamically noise activated in much the same manner as the Miller effect in Amplifiers, the large signal, DC-Link or Reservoir Capacitance will increase as the input noise increases, as shown in the Figure 12 through 17 data examples (1uF Static Capacitance in these examples). With moderate increases in noise levels above small signal (25mVpp), the on chip reservoir capacitance increases up to 600X of the nominal, static value.

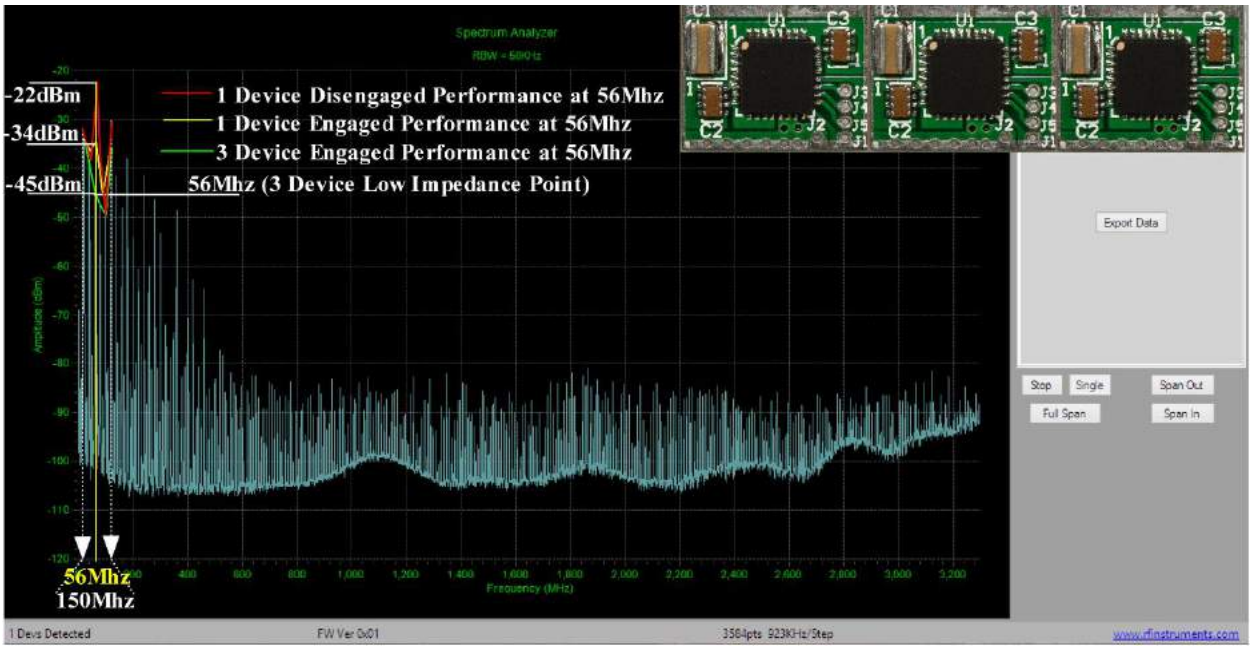


Figure 12: CC-100IP-MB Large Signal Reservoir Capacitance Dynamics

Figures 12 and 13 show the large signal behavior described above. Using the low impedance point shown for single, engaged CC-100IP-MB Chip, shown in Figure 12, as a baseline measurement, the lowest impedance point for 3 parallel connected CC-100IP-MB Chips, moves from 170Mhz to 56Mhz(a factor of 3 reduction in frequency) and a ~ 6 to 7 dB magnitude reduction is realized.

Figures 12 and 13 show a supply noise spectrum generated by the Pseudo Random Test IC for 3 parallel connected CC-100IP-MB Chips. Figure 13 shows a close up of the lowest impedance point (56Mhz), the **green** curve superimposed on the spectral noise plot showing the effect of the 56Mhz low impedance point on the overall noise spectrum for the 3 engaged parallel CC-100IP-MB Chip instances. As Figures 12 and 13 show, the magnitude of the frequency content at 56Mhz for the 3 parallel CC-100IP-MB instances is -45dBm.

The **yellow**, 56Mhz superimposed curve in Figures 12 and 13 shows the magnitude of the frequency content centered at 56Mhz for one engaged CC-100IP-MB Chip. As shown in Figure 11, the single chip lowest impedance point moves to 170Mhz, thus the magnitude of the spectrum centered at 56Mhz moves up ~12 dB to -34dBm.

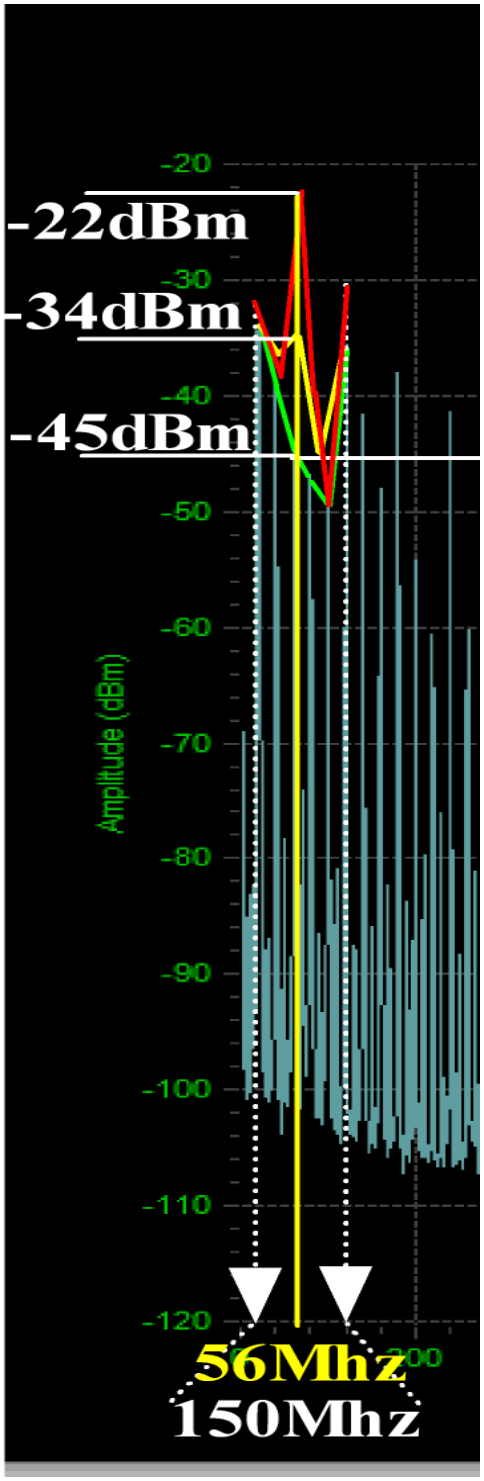


Figure 13: Large Signal Dynamics

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The **red**, 56Mhz superimposed curve in Figures 12 and 13 shows the magnitude of the frequency content centered at 56Mhz for one disengaged CC-100IP-MB Chip. As shown in Figure 10, the disengaged, single chip lowest impedance point moves to 370Mhz, thus the magnitude of the spectrum centered at 56Mhz moves up another ~12 dB to -22dBm.

Thus, the spectrum data shown in Figures 12 and 13 yield an additional 6dB drop on top of the nominal small signal 6db magnitude reduction shown with the small signal network analysis in Figures 10 and 11. This additional 6 dB spectral magnitude reduction is the result of supply line noise magnitudes greater than small signal (noise magnitude 50 mVpp in this case), and is caused by the inherent energy harvesting occurring within the CC-100 device. This behavior is reflective of a DC-Link or reservoir capacitance increase that is resultant of higher than small signal noise magnitudes (25mVpp) being input to the device from the supply line. Since dynamic reservoir capacitance does not behave in the same manner as nominal capacitance (generally, the larger the nominal capacitance, the lower in frequency the capacitive response becomes), greater capacitive cancellation and reservoir effects are seen to increase as supply line noise signal increases.

The rms delta in current shown in the Figures 12 and 13 plots is 3.45mA, that ranging from the disengaged **red** curve to the 3 parallel engaged devices (the **green** curve). Thus, the larger the noise input magnitude with the CC-100IP-MB, the greater the reservoir effects become.

Figures 14 and 15 show CC-100 response to a high power impulse and the resulting increased reservoir capacitance effect (Figures 12 and 13) as supply line noise increases. As the Figure 14 and 15 plots show, a 142mA delta exists between the disengaged and engaged impulse response plots, Figures 16 and 17 showing the scaling that exists between the device input current and reservoir capacitance the CC-100IP-MB generates. Thus, with greater noise magnitudes on system supply lines, the CC-100IP-MB outputs greater reservoir currents to cancel the noise impulses that are input to the IP

The mathematics for this reservoir effect are simple

Equation 3:

$$Ic = C(\frac{dv}{dt})$$

Rearranging:

$$\frac{Ic}{\frac{dv}{dt}} = Creservoir$$

For the CC-100IP-MB test chip case:

$$\frac{Ic}{250} = Creservoir$$

The dv/dt substitutions above are generated from confidential CC-100 device parameters

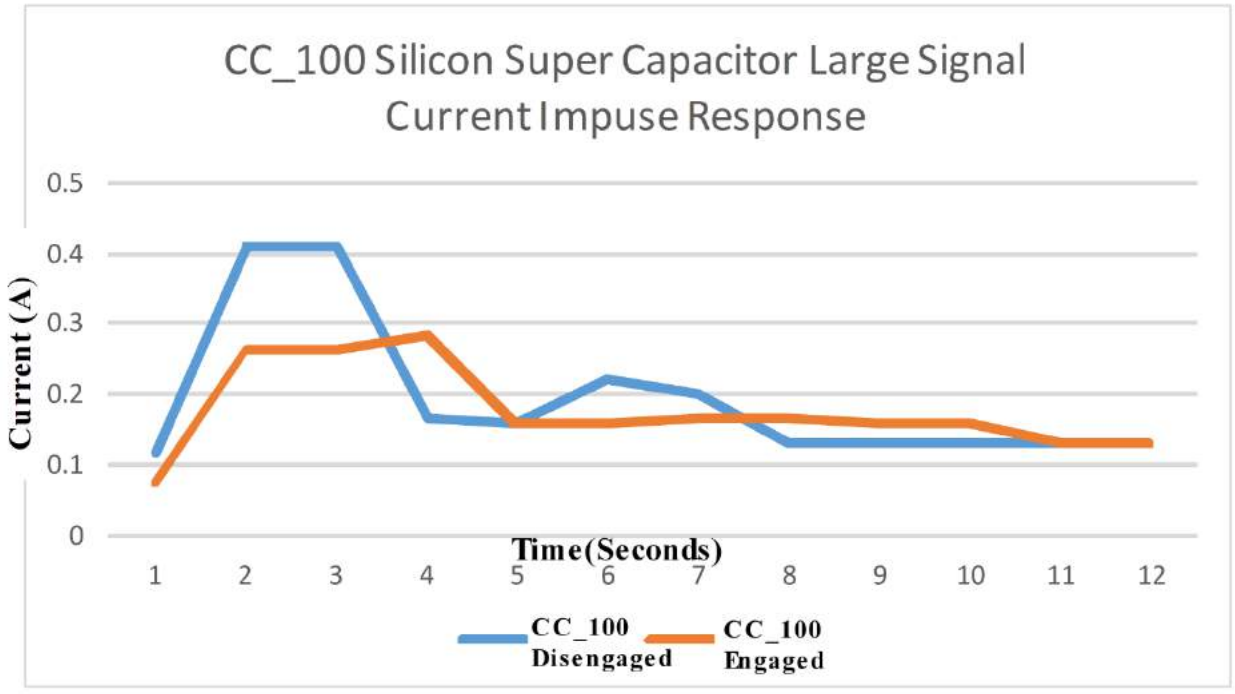

Figure 14: CC-100IP-MB IP Disengaged/Engaged High Current Impulse Response

Figure 14 shows the CC-100IP-MB (Silicon Super Capacitor Effect) response to high current impulses. The **blue** plot in Figure 14 shows a typical system response to an increased load current demand from system regulators. Not only is the CC-100 disengaged impulse magnitude higher than the **brown** CC-100IP-MB engaged plot in Figure 14, the disengaged plot shows a higher degree of ringing, moving toward an underdamped system response, with respect to the

engaged plot. The Figure 14 plot also shows the effect of the negative feedback of the energy harvesting embedded in the CC-100IP-MB and it's effect on system stability. The CC-100IP-MB injects recharging current in response to the supply line voltage perturbation that is the result of system load current increases, effectively canceling a portion of the initial induced supply line voltage disturbance. One could also say that the increased reservoir capacitance from the CC-100IP-MB does a better job of filtering the result of instantaneous load current increases.

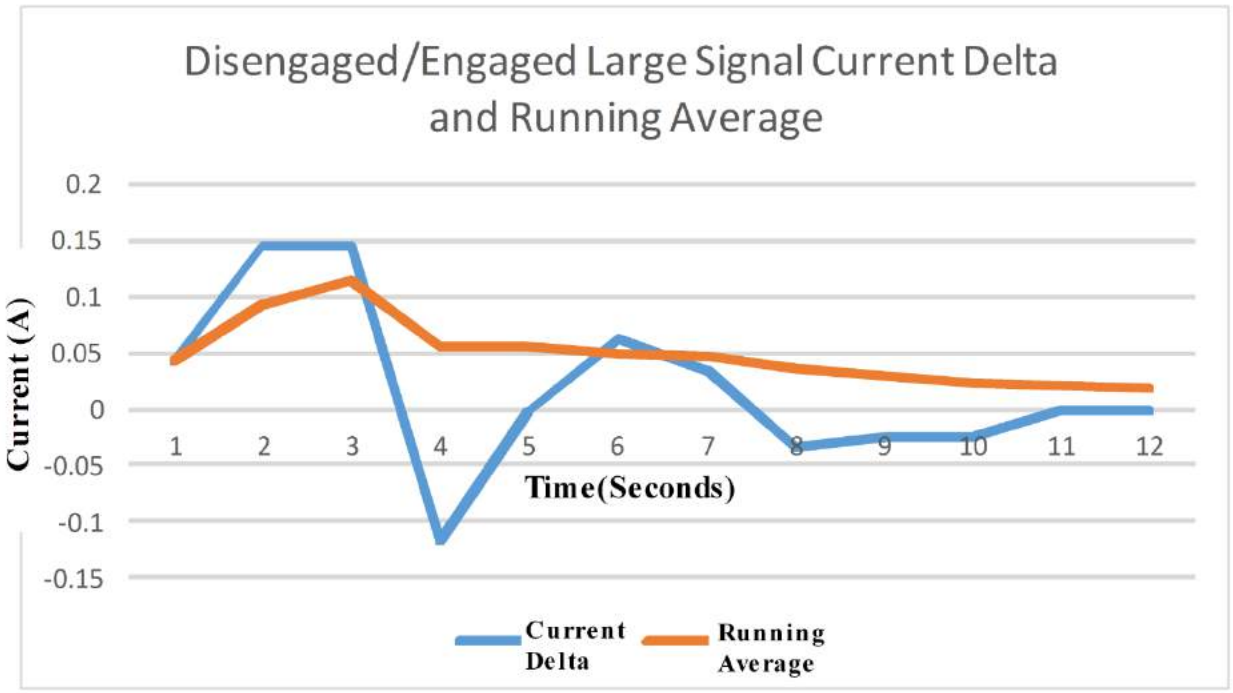

Figure 15: CC-100IP-MB Current Delta with Running Average

Figure 15 shows the current disengaged/engaged delta and running current delta average for the Figure 14 plots. The positive excursions above zero current in Figure 15 is the result of current injected from the CC-100IP-MB IP to cancel the induced voltage perturbation and supply the current created by the load current impulse demanded by the circuit load, the negative excursions below zero current in the plot. The result of supply line ringing in response to the initial current impulse from the circuit load. One will notice that the current delta finally settles to zero current after 11 seconds, showing that the CC-100IP-MB responds only to dynamic current perturbations, and the running average showing an overall positive current and power savings.

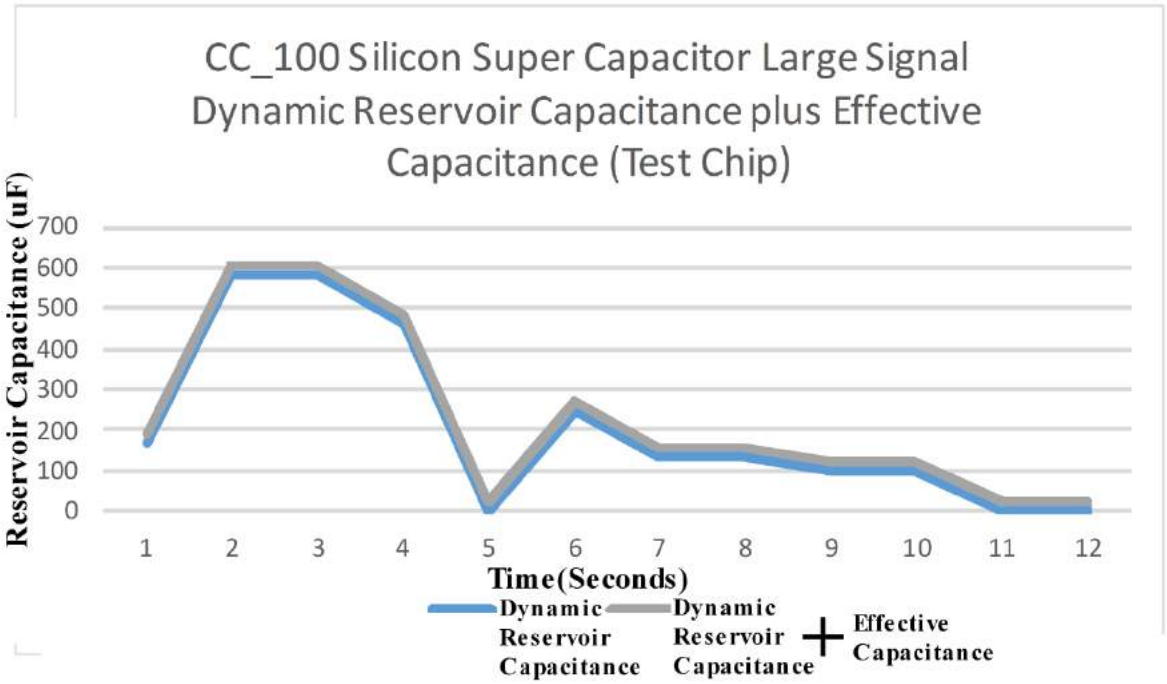

Figure 16: CC-100IP-MB Test Chip IP Dynamic Reservoir plus Effective Capacitance Test Chip Performance (1uf Static Output Capacitance)

Figure 16 shows the total CC-100IP-MB Test Chip IC dynamic reservoir and effective capacitance increases (Silicon Super Capacitor Effects) that are the result of the load current impulses imposed on the System Cap_in terminal of the CC-100IP-MB Test Chip IC. The **grey** curve is the combination of the dynamic reservoir and effective capacitance, or total capacitance that the CC-100IP-MB generates in response to high current impulses, the **blue** curve is the dynamic reservoir capacitance alone. As one can see, the dynamic reservoir capacitance magnitude far outweighs the effective capacitance, and the dynamic reservoir capacitance driven by the magnitude of input dynamic current and Cap_in perturbations.

With a 1uF static output or return capacitance used on the CC-100IP-MB Test Chip IC, the magnitudes of the reservoir capacitance approach 1mF. This is an order of magnitude increase with respect to the capacitance provided by standard MLCCs. This is a good example of how the CC-100IP-MB Test Chip IC and IP block can dynamically enhance supply bypassing at the PCB and integrated circuit level of integration.

So**,** the 2X increase in small signal effective capacitance, the dynamically controlled increases in large signal, reservoir capacitance, the 25% system reduction in ESL, and the resulting 20% to 36% drop in overall Dynamic Current and Power Draw, leads to better high frequency (lower ESL) and low frequency, higher Effective and Reservoir Capacitance—enhancing system DC-Link Capacitance, leading to better filtering capability with Power Reduction from System Batteries.

CC-100IP-MB Behavioral Model

To facilitate easy integration of the CC-100IP-MB into new designs, CurrentRF has created an easy to use behavioral model that can be dropped into the top level of Electric Vehicle designs.

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Figure 17 shows the schematic details of the CC-100IP-MB IP Behavioral Model. The CC-100IP-MB Behavioral Model is built from Standard Spice components found in any Spice based simulator (Cadence, Mentor Graphics, Silvaco/SmartSpice, etc.). The W0 Switch and GG1 VCCS parameters can be changed for maximum CC-100IP-MB performance and applied to the Figure 18 System Test Bench.

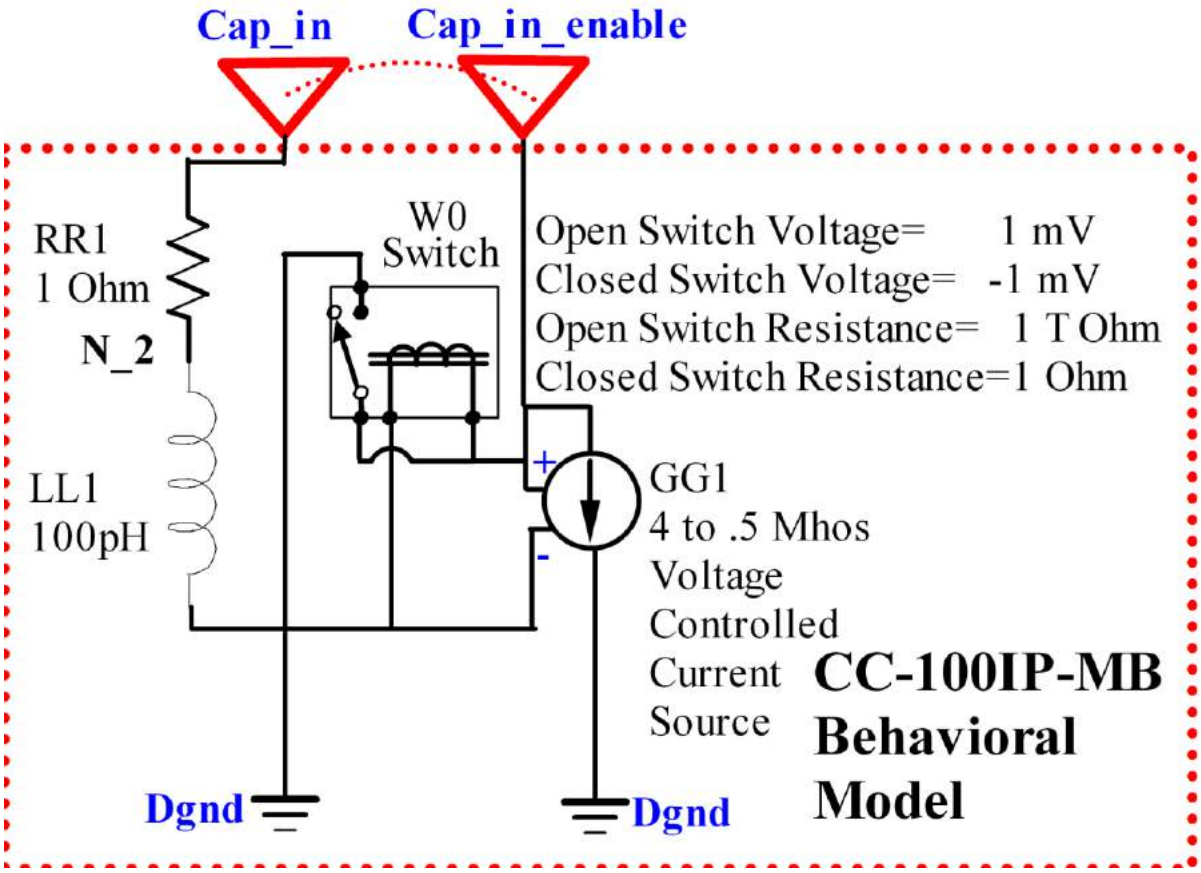


Figure 17: CC-100IP-MB Behavioral Model Schematic

CC-100IP-MB Top Level Test Bench

Figure 18 shows the schematic details of the CC-100IP-MB top level evaluation test bench. The stimulus, applied at the EV System Supply Port, Is intended to be Traction and/or Controller Ripple applied to the Input DC-Link or Reservoir Capacitor. The W0 Switch and GG1 VCCS parameters can be changed for maximum CC-100IP-MB performance and applied to the Figure

18 System Test Bench. These final parameters should be communicated to CurrentRF, as they will guide the structure of the finial Silicon IP design.

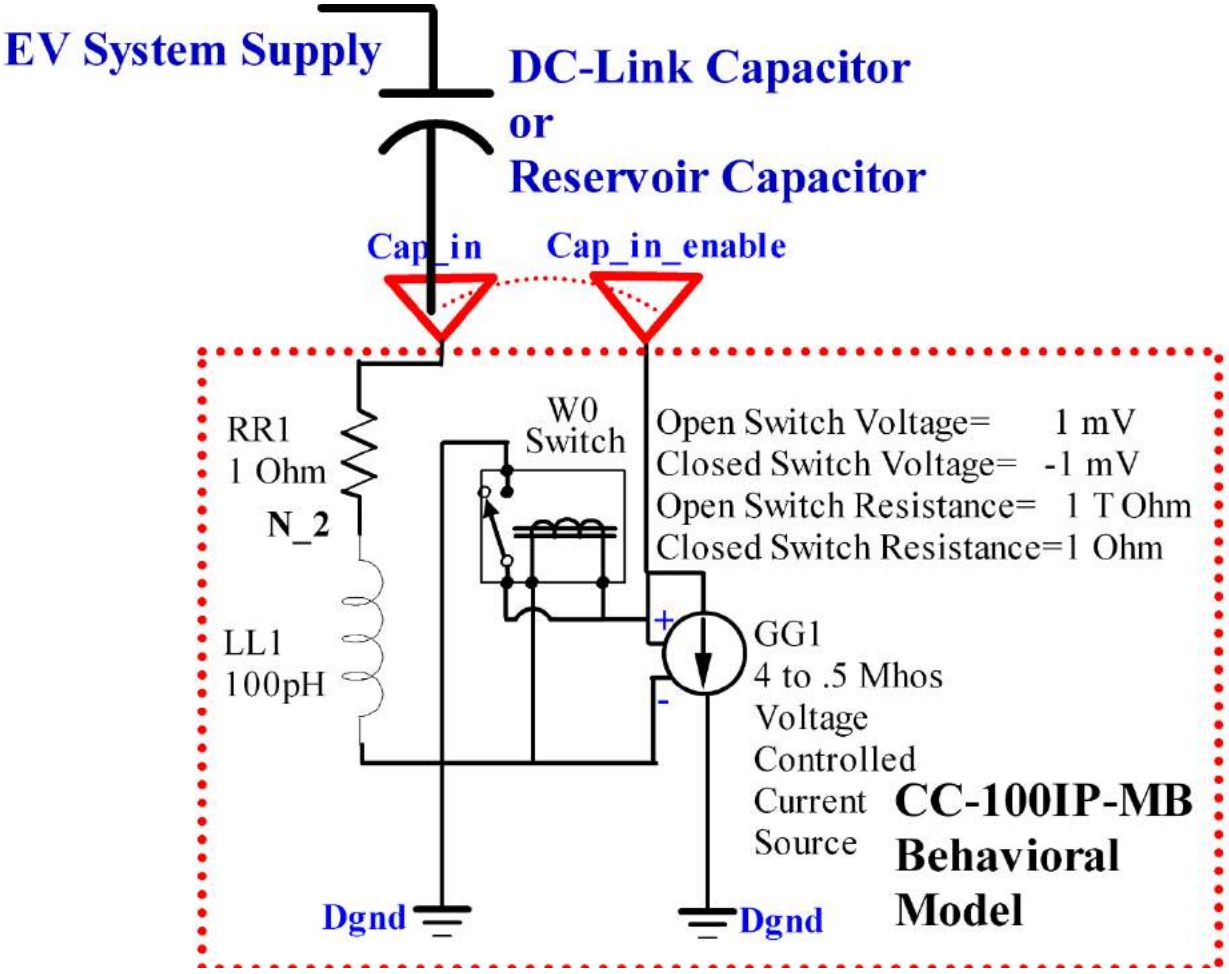
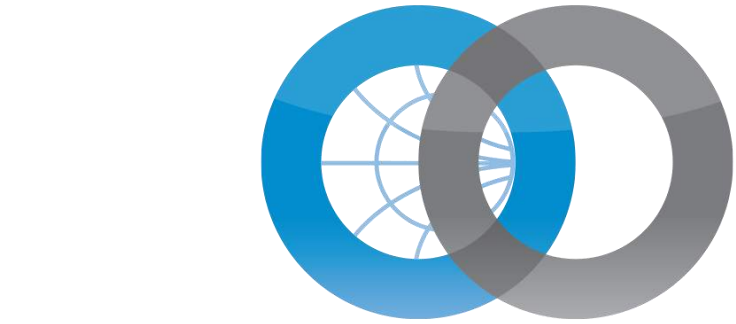


Figure 18: CC-100IP-MB Behavioral Model Schematic and Top Level Circuit Test Bench

Based on Simulation results with the behavioral model shown in Figures 17 and 18, the CC-100 IP-MB can be customized for device sizing for any application and desired process node. Contact CurrentRF for details.

For additional technical or ordering information contact us at:



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