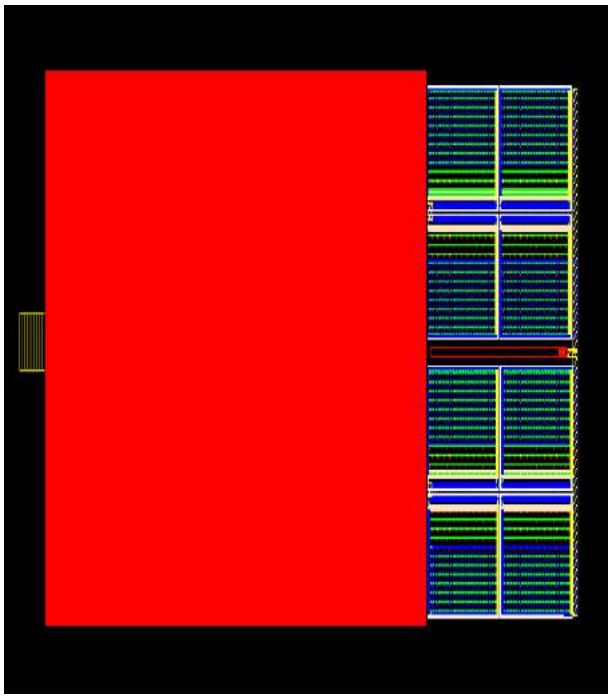


CC-100IP-RF-RF Sensitivity IP
Reduces RF Supply Line Noise-Increasing RF Amplifier Sensitivity
Up to 600X Effective Capacitance Increase
Dynamic Control of Reservoir Capacitance
25% Effective Series Inductance Reduction
On-Chip Cybersecurity Enhancement
Customized-On-Demand IP (Quick Turn Around)

General Description

The CC-100 IP is a Hyper-decoupling capacitor with a Capacitance Multiplication, Series Inductance Nullification, Cybersecurity Enhancement and an Energy Harvesting capabilities. The Hyper-Bypass Capacitor IP creates the lowest Impedance point in IC power grids aiding in maximum on chip supply line filtering, showing an up to a 600X improvement in effective and reservoir capacitance. The IP features a circuit noise activated dynamic input current controlled reservoir capacitance, and can function as a “stand-alone” on Chip DCAP, or work in parallel with existing DCAP structures. Due to the negative feedback embedded in the IP, the CC-100 features a 25% reduction in Hyper-Capacitor effective series inductance (ESL). The IP operates by feeding back a portion (nominally 20%) of the bypass current flowing through IP input base capacitors, feeding back current onto the chip power grid, preventing bypass Capacitor Deep discharge, and thus Deep recharge from system supplies, thus reducing overall chip dynamic power draw. These effects substantially reduce RF Emissions from chip power grids making systems less vulnerable to cyber hacking and more secure. The IP draws no current for operation, thus maximizing block efficiency.

The Hyper Cap IP is meant to replace or work in parallel with existing on chip decoupling capacitors, thus can be shaped into various aspect ratios and sizes to fit on-chip “white space”, the area under power grids, etc. in the same fashion as typical on-chip decoupling capacitors. In similar fashion to typical decoupling capacitors, the IP blocks can be connected in parallel to increase overall RF emission reduction, reservoir capability, and effective capacitance.

Topology

Ultra-Low Impedance Input Design
Single High Impedance Output
Bi-Directional Bypass Operation
Proprietary/Patented Topology

Features

On-Chip Cybersecurity Enhancement
Dynamic Reservoir Cap Power Reduction
600X Increase in Effective Capacitance
25% Reduction in Capacitor ESL

Functional Description

c The CC-100IP is a Hyper decoupling capacitor with embedded feedback which is activated by dynamic noise current applied to it's Dvdd supply terminal. The embedded feedback creates conditions in which capacitive filtering is enhanced, normally thrown away current is recycled recycled, and ESL is reduced, thus creating the lowest impedance point for noise in IC Power Grids.

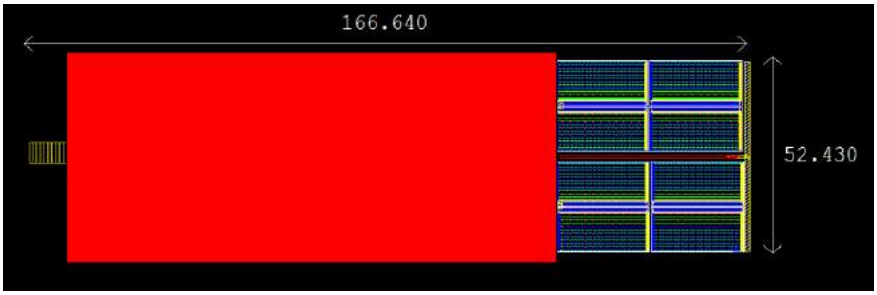
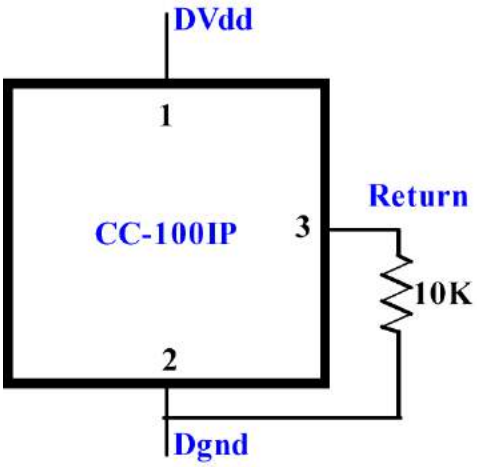


Figure 1: Typical CC-100IP Aspect Ratio

Figure 1 shows the typical footprint of the CC-100IP. Figure 1 shows a 166um X 53um rectangular aspect ratio footprint. The IP block can be configured into almost any aspect ratio, giving it maximum versatility and flexibility in customer designs.

The IP is designed to be placed into the "white space" on chips and under supply line power busses, in the same manner as typical on-chip DCAPs are utilized.



Symbol	Pin	Type	Description
Dvdd	1	Power	Supply
Dgnd	2	Power	Ground
Return	3	Signal	Output Bias
			(Connect to 10K
			on-Chip Resistor)

Figure 2: CC-100IP Block Diagram and Pinout

Figure 2 shows the CC-100IP cell and pinout. Three connections are all that is needed for IP block operation. Dvdd and Dgnd are identical in function to conventional DCAPs. The return pin is connected to a 10K ohm on-chip bias resistor, the opposite end of the resistor connected to Dgnd.

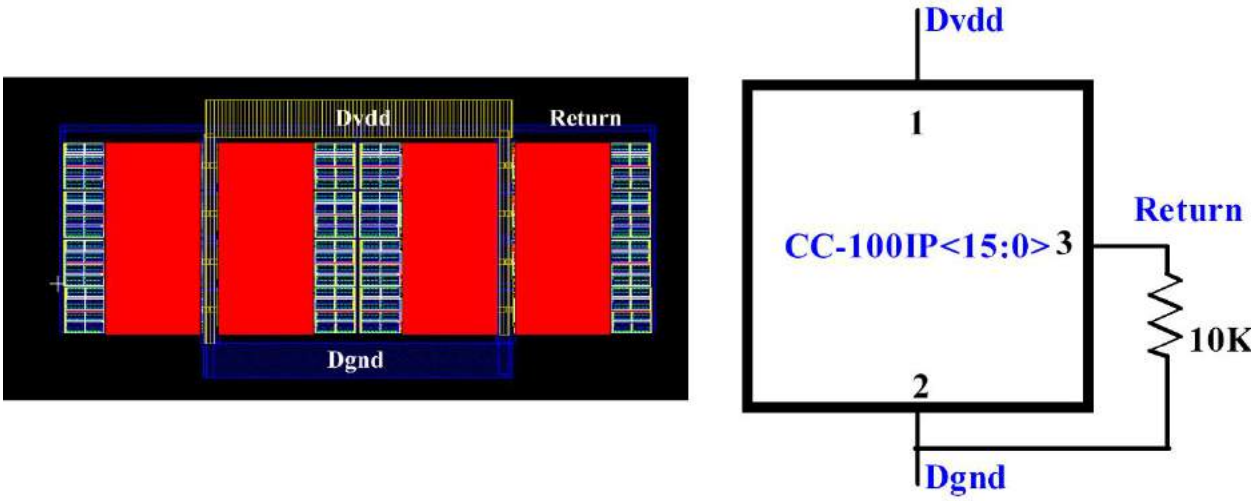


Figure 3: CC-100IP Arrayed Cell Example and Block Diagram

Figure 3 shows how CC-100IP cells can be connected in an arrayed grid pattern, forming a large, composite bypass capacitor. In this example, sixteen CC-100IP cells are connected in parallel forming a composite, large, on-chip bypass capacitor.

Connecting the IP is this fashion does not degrade the benefits gained from the single IP block of Figures 1 and 2 (benefits shown in Table 1). Connecting the IP blocks in parallel, as in Figure 3, the IP benefits are preserved, with the added benefits of reservoir, effective, and static capacity increases (see Figure 4), beyond that of any typical bypass capacitor. A single on chip 10K resistor is all that is needed for biasing all the CC-100IP blocks in the 16 block array and is scalable for any CC-100IP array of any size.

Static/Dynamic Characteristics

Small Signal Effective Capacitance Behavior

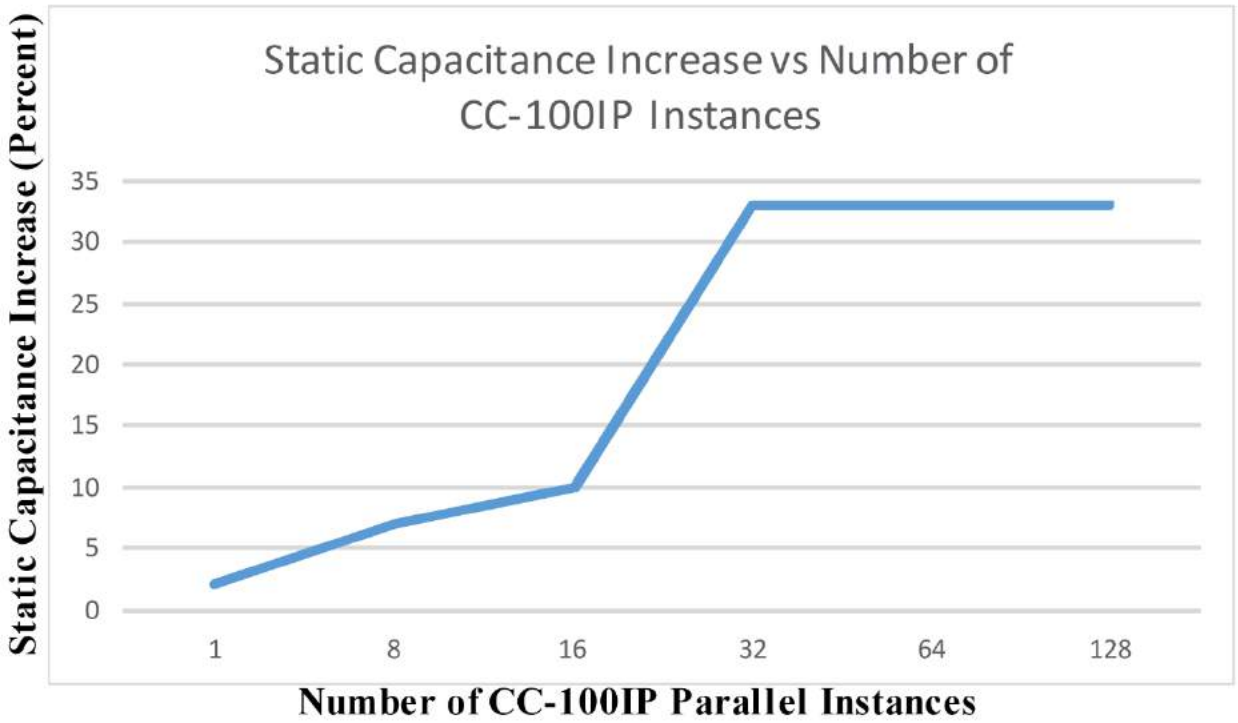


Figure 4: Static, Small Signal, Effective Capacitance Increase with Composite, Parallel CC-100IP Instances

Static, Small Signal, Effective Capacitance is shown to increase from 2% to 33% with respect to standard DCAPs, as the number of parallel CC-100IP instances is increased from 1 to 32, as shown in Figure 4. Beyond 32 parallel CC-100IP instances, a maximum limit of a 33% small signal,effective capacitance increase with respect to standard DCAPs is seen. The data in Figure 4 was taken from the CC-100IP implemented on Jazz Semiconductors' CA18 CMOS process.

This static capacitance increase is due to the dynamic, return current action of the CC-100IP and is seen to increase beyond 33% as higher levels of dynamic current is applied to the Dvdd terminal of the IP block. The data shown in Table 1 below shows this phemomenon.

IP/Cap Comparision Table	CC-100 IP Static Performance	CC-100 IP Dynamic Performance	CC-100 IP Performance Enhancement
Effective Series Inductance	100ph	75ph	25% ESL reduction vs standard DCAPs
Effective Capacitance	16pf	32pf	2X Increase in Effective Capacitance
Actual Capacitance Scaling	1X	1x	No Change in Actual Dimensions
Dimensions (square um)	45	45	No Change in Actual Dimensions

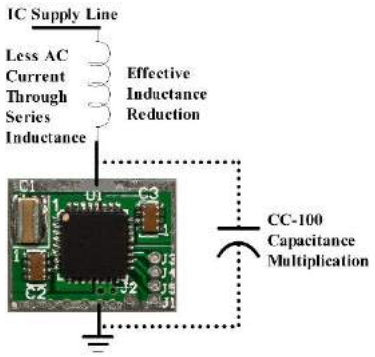
Table 1: CC-100IP Static/Small Signal, Dynamic Performance with respect to Standard DCAPs

Table 1 shows the static characteristics of the CC-100IP and the dynamic benefits of using this IP in the place of standard, on-chip. MOS capacitors. Given the aspect ratio of the CC-100IP

shown in Figure 1 (45 square microns--the approximate area underneath the red block in Figure 1) the Effective Series Inductance (ESR) is 100pH. When the CC-100IP is dynamically activated, the ESR of the IP drops by 25%, to 75pH in this example.

Small Signal Broadband Impedance--Broadband Frequency Response

Silicon Proven CC-100 Test Chip IP, shown to the right, of which the CC-100IP is a base component, Figures 5 and 6, 8 through 13 show CC-100IP CMOS7RF (Global Foundries) AC characterization. Inductance Nullification and Capacitance Multiplication creates the lowest impedance point in the system.



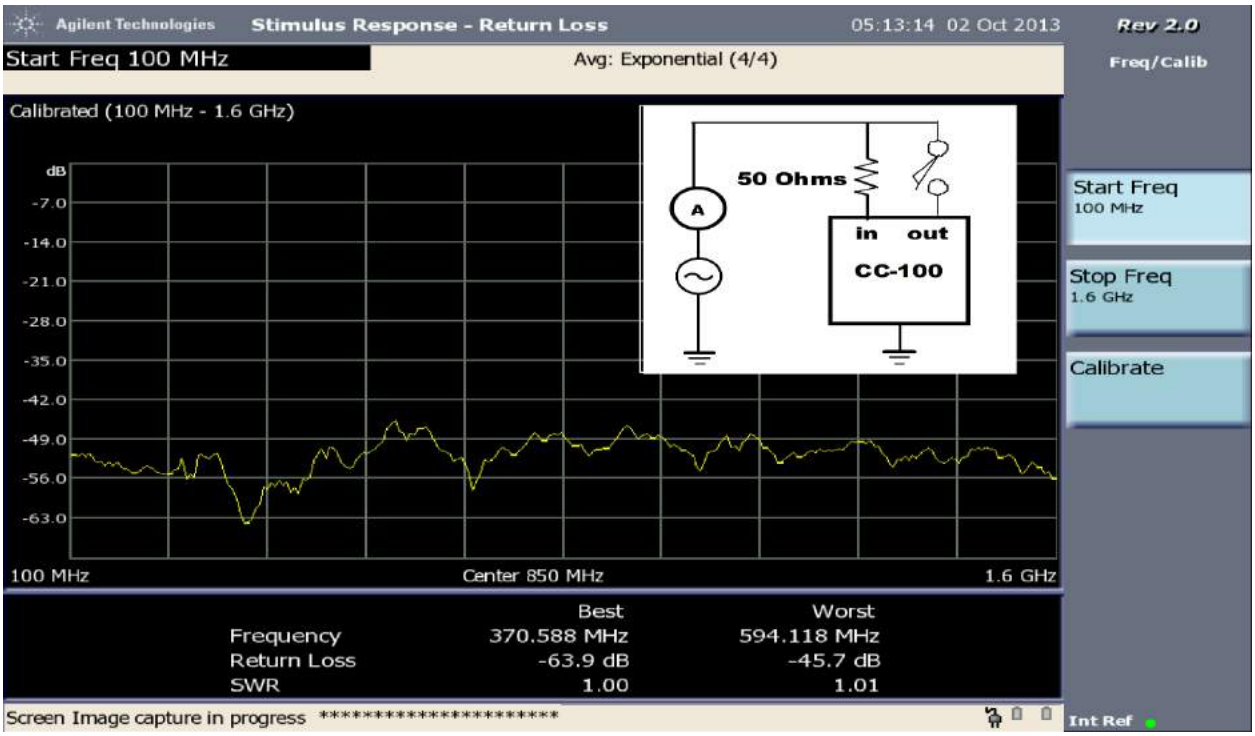


Figure 5: CC-100IP Small Signal S11 Input Plot (CC-100IP Disengaged)

The S_{11} return loss plot in Figure 5 graphically displays the bandwidth, input impedance, EMI suppression, and spectral response of the CC-100 Test Chip IP. The plot in Figure 5 shows a CC-100IP bandwidth ranging from 100Mhz to 1.6Ghz and the wideband S_{11} return loss of the device. With a series 50 Ω resistor placed at the input of the device, as seen in Figure 5, the overall VSWR of the device input is quite good, varying from nearly perfect, VSWR of 1.0 at 370Mhz, to a worst case VSWR of 1.01. The Figure 5 plot shows that the low input impedance of the device is negligible to the total input resistance, and does not show much variation over the input bandwidth of the IP.

In Figure 5, with the CC-100IP disengaged, looking exclusively into the 11uF input base capacitance in this example, the best return loss/SWR and the lowest impedance point occurs at 370Mhz (-64dB) and corresponds to a capacitive low impedance magnitude of 39 Micro Ohms. A short math proof is as follows.

Equation 1:

$$50 * invlog\left(-\frac{dB}{10}\right) \cong 1/(2 * \pi * f * C)$$

Using the CC-100IP data, the lowest impedance point frequency in the Figure 5 plot, as well as the "Best" return loss and SWR numbers from the Network Analyzer, gives

$$50 * invlog(-\frac{63.9dB}{10}) \cong 1/(2 * \pi * 370Mhz * 11uF)$$

Solving yields

$$20\mu\Omega \cong 39\mu\Omega$$

Which, within measurement and error tolerances, the results are essentially equal.

Narrowband spectral peaks and dips remain, however, in Figure 5, indicative of imperfections in the matching of the power grid on the IP evaluation board, test system cabling, and connectors.

The plot in Figure 6 shows the S_{11} spectral results of the CC-100IP's negative feedback and power grid compensation. The Figure 6 plot demonstrates an increase in overall "returned" current (a 7 dB decrease in return loss, a slightly higher worst case VSWR of 1.03 vs. 1.01), but much reduced spectral peaks and dips, with respect to the plot in Figure 5. This return loss and VSWR decrease is not due to typical load mismatch effects, but is the result of CC-100IP action, returning current to the system for reuse. Thus, in the plot in Figure 6, the network analyzer power detectors show the device current return and negative feedback compensating for the imperfections present in the power grid on the CC-100IP evaluation board, test system cabling, connectors, etc.

Using the same example base input capacitance, 11uF, as in the Figure 5 plot, and engaging the CC-100IP, the best return loss/SWR the transfer function lowest impedance point is translated down to 170Mhz(-56.3dB), as seen in Figure 6. Accounting for a +7 dBm scaling with respect to the Figure 5 plot, this due to return currents flowing from the CC-100IP output into the Network Analyzer detectors, the low impedance point corresponds to a capacitive low impedance of 42 Micro Ohms. This low impedance dip in Figure 6 fits the impedance and frequency characteristic that would be seen utilizing a standard 22uF capacitance. This measurement confirms the effective capacitance increase generated by the action of the CC-100IP. The math for this condition as follows.

Equation 2:

$$50 * invlog((-dB - 7dB)/10) \cong 1/(2 * \pi * f * C)$$

Using the CC-100IP data, the lowest impedance point frequency in the Figure 6 plot, as well as the “Best” return loss and SWR numbers from the Network Analyzer gives

$$\left(50 * invlog\left(\frac{(-56.3dB-7dB)}{10}\right)\right) \cong 1/(2 * \pi * 170Mhz * 22uF)$$

Solving yields

$$23.4\mu\Omega \cong 42\mu\Omega$$

Which, within measurement and error tolerances, the results are essentially equal.

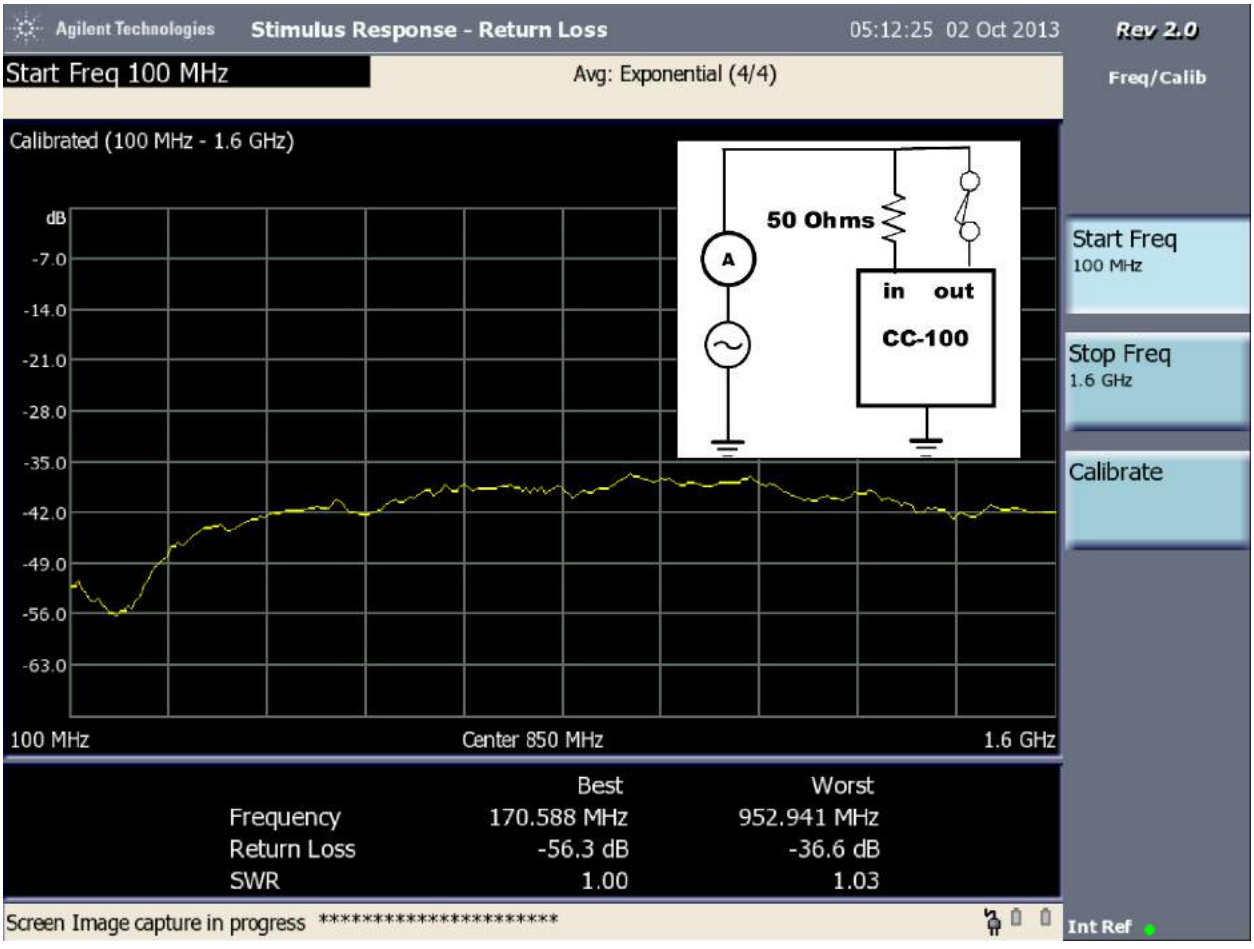


Figure 6: CC-100IP Small Signal S11 Plot (CC-100IP Engaged)

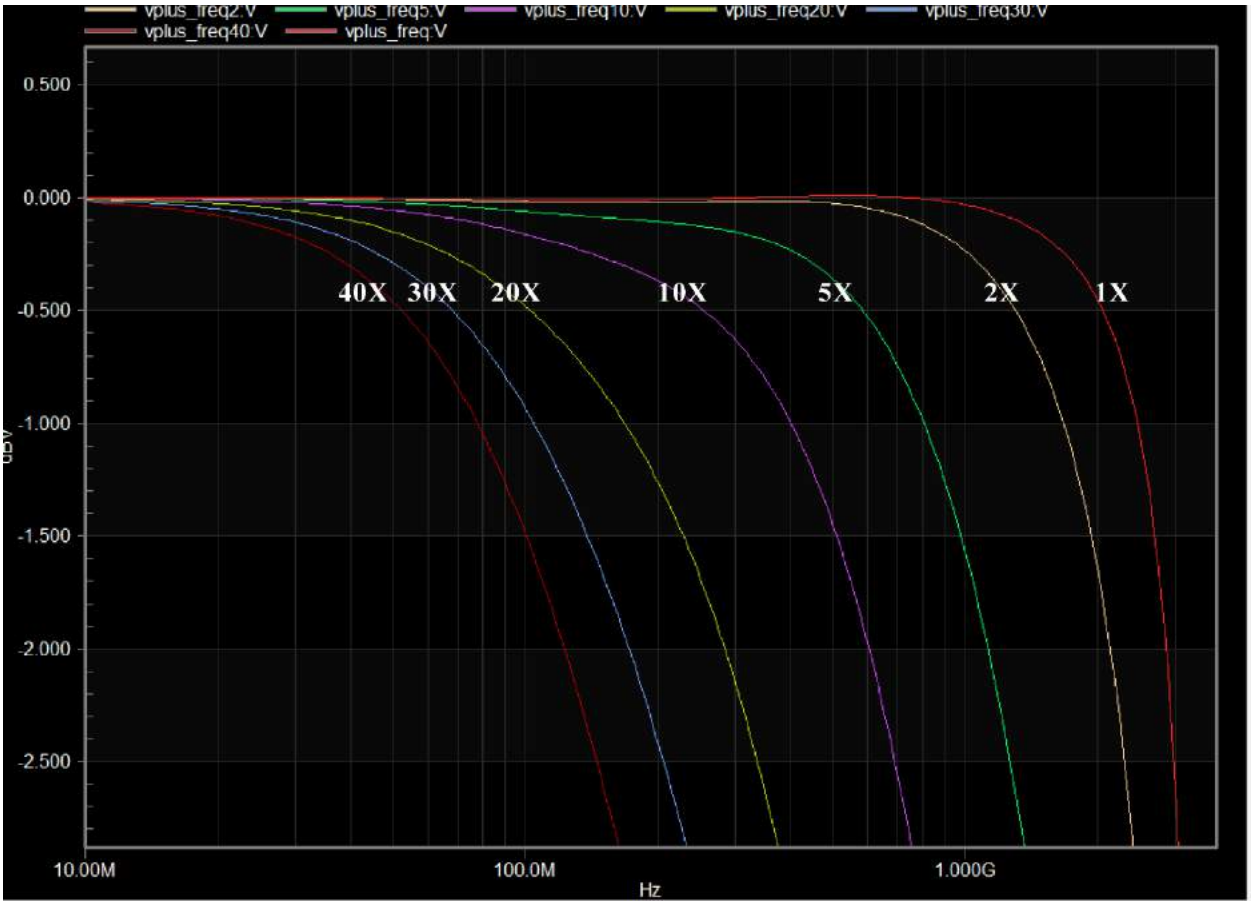


Figure 7: CC-100IP Filter Bandwidth with respect to multiple, parallel instances

Figure 7 shows the effect of paralleling multiple CC-100IP instances on the filtering bandwidth of the CC-100IP. This effect is similar to what is seen with standard DCAPs, the higher the capacitance, the lower the effective bandwidth of the filtering action and the higher rejection of on chip high frequency noise. The big advantage with the CC-100IP vs typical DCAPs is that as more CC-100IP blocks are placed in parallel, the effective and reservoir capacitance increases in accordance with the data taken in Figures 4, 8 through 10, and Table 1, RF emissions are suppressed and reduced, and up to 20% reduction is dynamic current and power drawn from the system supply is seen. The data in Figure 7 is based on a static 16pF unit cell capacitance, ported and implemented on Jazz Semiconductor's CA18 CMOS manufacturing process, embedded in the 45 square micron area of the CC-100IP block shown in Figure 1.

Large Signal Reservoir Capacitance Behavior

In the presence of curicut noise, CC-100IP Reservoir Capacitance increases up to 600X tracking input noise magnitude. As the dynamic current applied increases, the reservoir capacitance increases. With no dynamic current applied, the reservoir capacitance of the 45 square micron CC-100IP shown in the Figure 1 block is about 16pF, what one would get from Standard on-chip DCAPs. When dynamically activated, the large signal, reservoir capacitance will increase as the input noise increases, as in the Figure 8 and 9 and 10 through 13 data

examples. With moderate increases in noise levels above small signal (25mVpp), the on chip reservoir capacitance increases up to 600X of the static value.

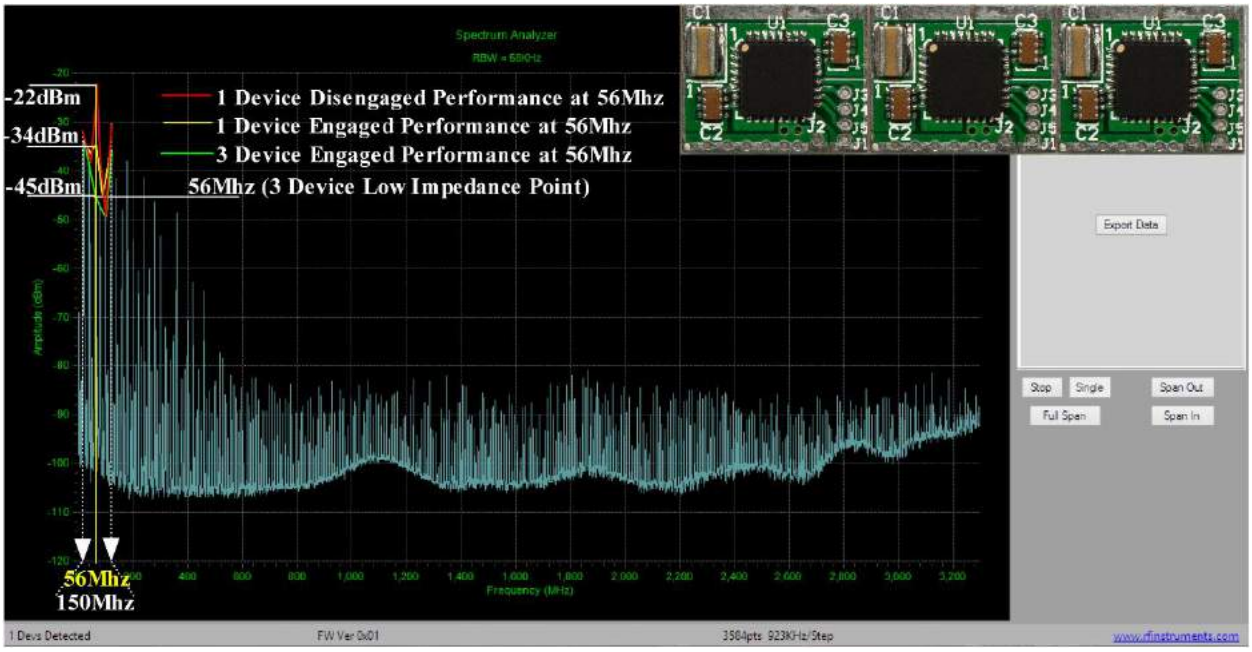


Figure 8: CC-100IP Large Signal Reservoir Capacitance Dynamics

Figures 8 and 9 show the large signal behavior described above. Using the low impedance point shown for single, engaged CC-100IP Test Chip, shown in Figure 5, as a baseline measurement, the lowest impedance point for 3 parallel connected CC-100IP Chips, moves from 170Mhz to 56Mhz(a factor of 3 reduction in frequency) and a ~ 6 to 7 dB magnitude reduction is realized.

Figures 8 and 9 show a supply noise spectrum generated by the Pseudo Random Test IC for 3 parallel connected CC-100IP Chips. Figure 9 shows a close up of the lowest impedance point (56Mhz), the **green** curve superimposed on the spectral noise plot showing the effect of the 56Mhz low impedance point on the overall noise spectrum for the 3 engaged parallel CC-100IP Chip instances. As Figures 8 and 9 show, the magnitude of the frequency content at 56Mhz for the 3 parallel CC_100 instances is -45dBm.

The **yellow**, 56Mhz superimposed curve in Figures 8 and 9 shows the magnitude of the frequency content centered at 56Mhz for one engaged CC-100IP Chip. As shown in Figure 6, the single chip lowest impedance point moves to 170Mhz, thus the magnitude of the spectrum centered at 56Mhz moves up ~12 dB to -34dBm.

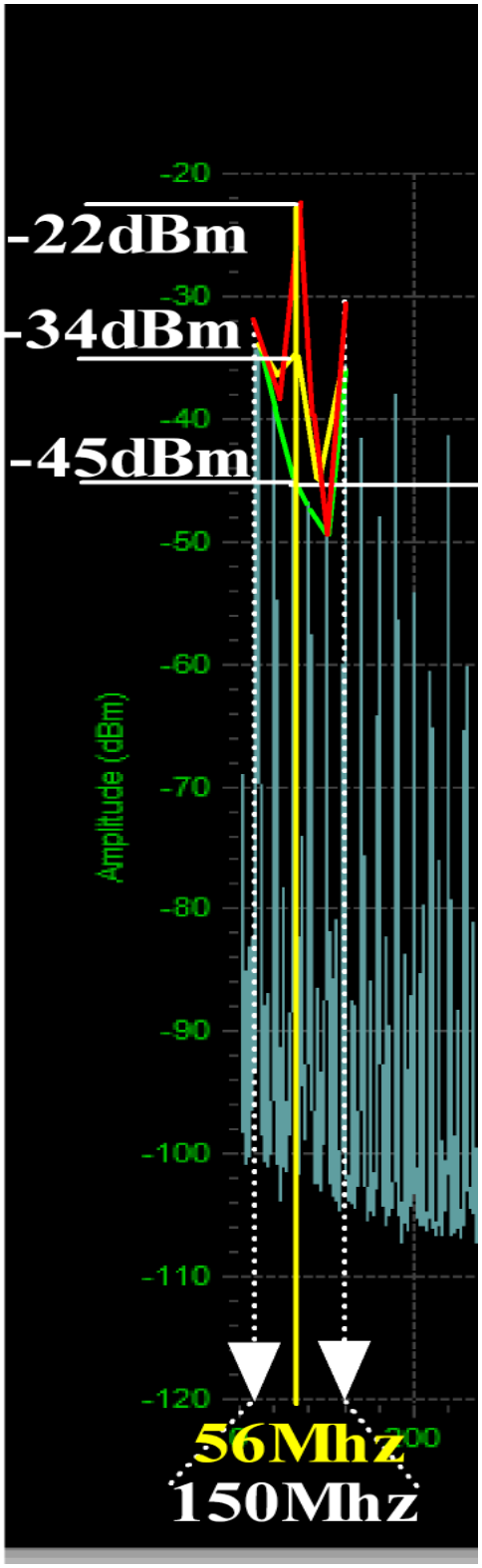


Figure 9: Large Signal Dynamics

The **red**, 56Mhz superimposed curve in Figures 8 and 9 shows the magnitude of the frequency content centered at 56Mhz for one disengaged CC-100IP Chip. As shown in Figure 5, the disengaged, single chip lowest impedance point moves to 370Mhz, thus the magnitude of the spectrum centered at 56Mhz moves up another ~12 dB to -22dBm.

Thus, the spectrum data shown in Figures 8 and 9 yield an additional 6dB drop on top of the nominal small signal 6db magnitude reduction shown with the small signal network analysis in Figures 5 and 6. This additional 6 dB spectral magnitude reduction is the result of supply line noise magnitudes greater than small signal (noise magnitude 50 mVpp in this case), and is caused by the inherent energy harvesting occurring within the CC-100 device. This behavior is reflective of a reservoir capacitance increase that is resultant of higher than small signal noise magnitudes (25mVpp) being input to the device from the supply line. Since dynamic reservoir capacitance does not behave in the same manner as nominal capacitance (generally, the larger the nominal capacitance, the lower in frequency the capacitive response becomes), greater capacitive cancellation and reservoir effects are seen to increase as supply line noise signal increases.

The rms delta in current shown in the Figures 8 and 9 plots is 3.45mA, that ranging from the disengaged **red** curve to the 3 parallel engaged devices (the **green** curve). Thus, the larger the noise input magnitude with the CC-100IP, the greater the reservoir effects become.

Figures 10 and 11 show CC-100 response to a high power impulse and the resulting increased reservoir capacitance effect (Figures 12 and 13) as supply line noise increases. As the Figure 10 and 11 plots show, a 142mA delta exists between the disengaged and engaged impulse response plots, Figures 12 and 13 showing the scaling that exists between the device input current and reservoir capacitance the CC-100IP generates. Thus, with greater noise magnitudes on system supply lines, the CC-100IP outputs greater reservoir currents to cancel the noise impulses that are input to the IP.

The mathematics for this reservoir effect are simple

Equation 3:

$$Ic = C(\frac{dv}{dt})$$

Rearranging:

$$\frac{Ic}{\frac{dv}{dt}} = Creservoir$$

For the CC-100 Test Chip case:

$$\frac{Ic}{250} = Creservoir$$

For the CC-100IP case:

$$\frac{Ic}{15625000} = Creservoir$$

The dv/dt substitutions above are generated from confidential CC-100 device parameters

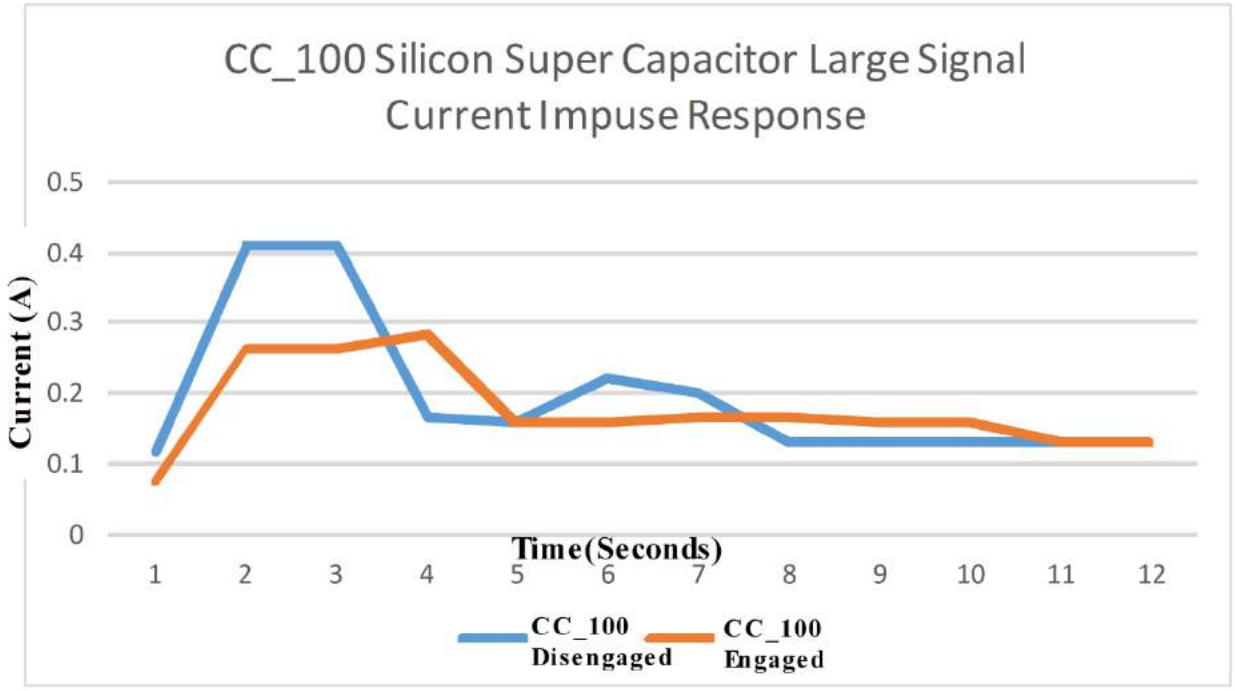


Figure 10: CC-100IP Disengaged/Engaged High Current Impulse Response

Figure 10 shows the CC-100IP (Silicon Super Capacitor) response to high current impulses. The **blue** plot in Figure 10 shows a typical system response to an increased load current

demand from system regulators. Not only is the CC-100IP disengaged impulse magnitude higher than the **brown** CC-100IP engaged plot in Figure 10, the disengaged plot shows a higher degree of ringing, moving toward an underdamped system response, with respect to the engaged plot. The Figure 10 plot also shows the effect of the negative feedback of the energy harvesting embedded in the CC-100IP and it's effect on system stability. The Silicon Super Capacitor function in the CC-100IP injects recharging current in response to the supply line voltage perturbation that is the result of system load current increases, effectively canceling a portion of the initial induced supply line voltage disturbance. One could also say that the increased reservoir capacitance from the CC-100IP does a better job of filtering the result of instantaneous load current increases.

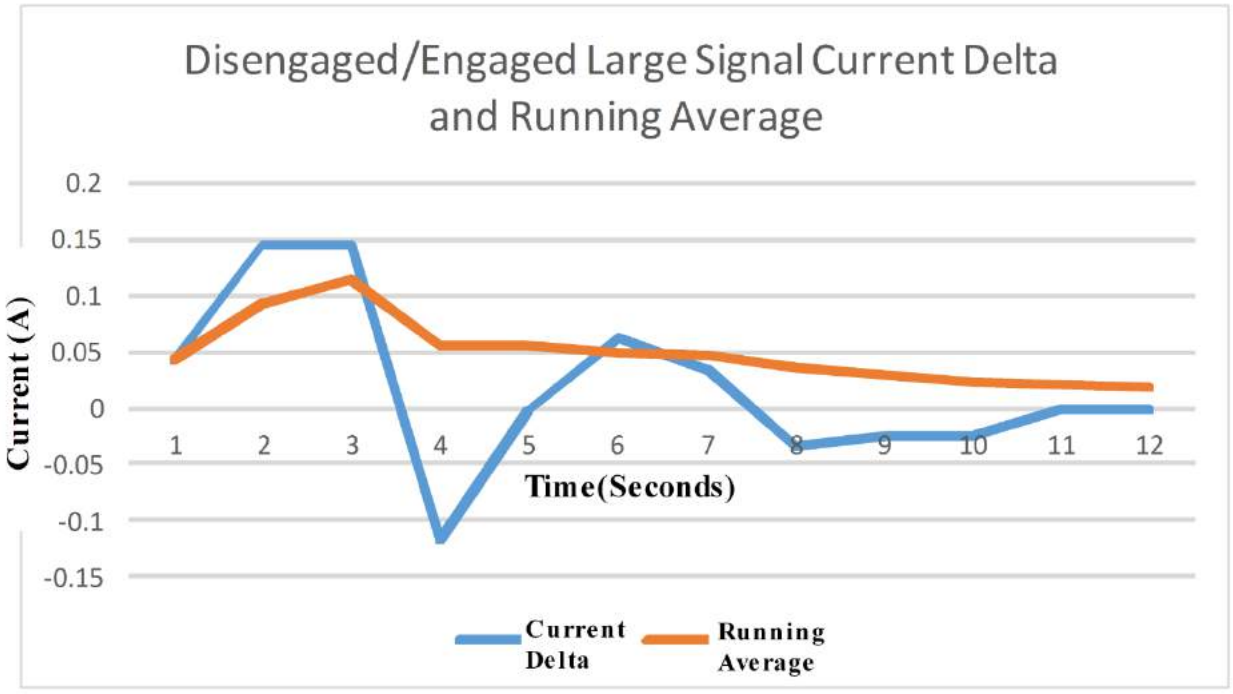


Figure 11: CC-100IP Super Capacitor IP Current Delta with Running Average

Figure 11 shows the current disengaged/engaged delta and running current delta average for the Figure 10 plots. The positive excursions above zero current in Figure 11 is the result of current injected from the CC-100IP to cancel the induced voltage perturbation and supply the current created by the load current impulse demanded by the circuit load, the negative excursions below zero current in the plot. the result of supply line ringing in response to the initial current impulse from the circuit load. One will notice that the current delta finally settles to zero current after 11 seconds, showing that the CC-100IP responds only to dynamic current perturbations, and the running average showing an overall positive current and power savings.

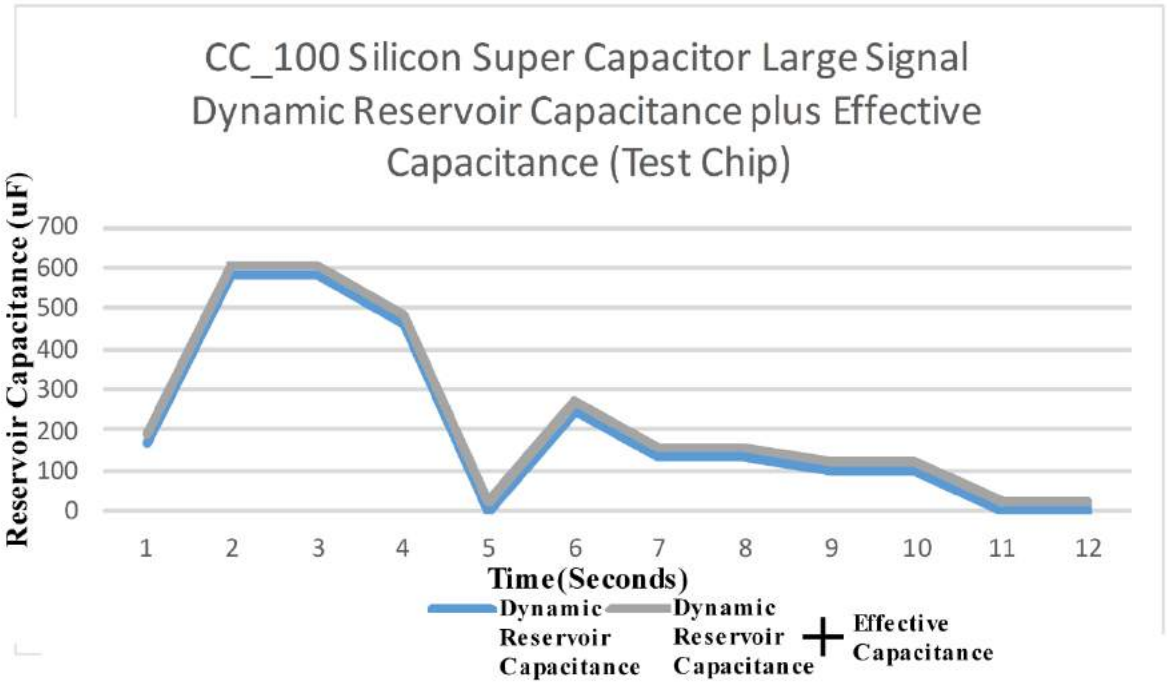


Figure 12: CC-100 Test Chip IP Dynamic Reservoir plus Effective Capacitance Test Chip Performance (1uf Static Output Capacitance)

Figure 12 shows the total CC-100 Super Capacitor Test Chip IP dynamic reservoir and effective capacitance increases that are the result of the load current impulses imposed on the system supply grid and the CC-100 Test Chip IP. The **grey** curve is the combination of the dynamic reservoir and effective capacitance, or total capacitance that the CC-100 generates in response to high current impulses, the **blue** curve is the dynamic reservoir capacitance alone. As one can see, the dynamic reservoir capacitance magnitude far outweighs the effective capacitance, and the dynamic reservoir capacitance driven by the magnitude of input dynamic current and supply voltage perturbations.

With a 1uF static output or return capacitance used on the CC-100 Test Chip, the magnitudes of the reservoir capacitance approach 1mF. This is an order of magnitude increase with respect to the capacitance provided by standard MLCCs. This is a good example of how the CC-100 Test Chip IC and IP block can dynamically enhance supply bypassing at the PCB and integrated circuit level of integration.

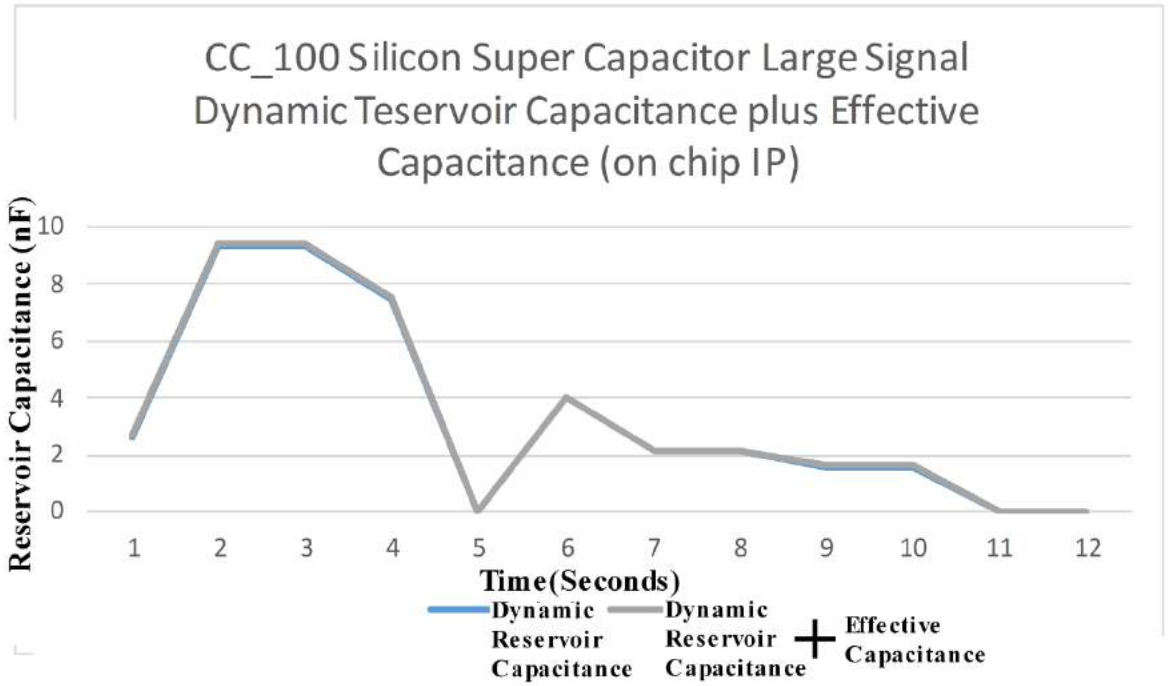


Figure 13: CC-100IP Dynamic Reservoir plus Effective Capacitance on chip IP Performance (16pf Static Output Capacitance)

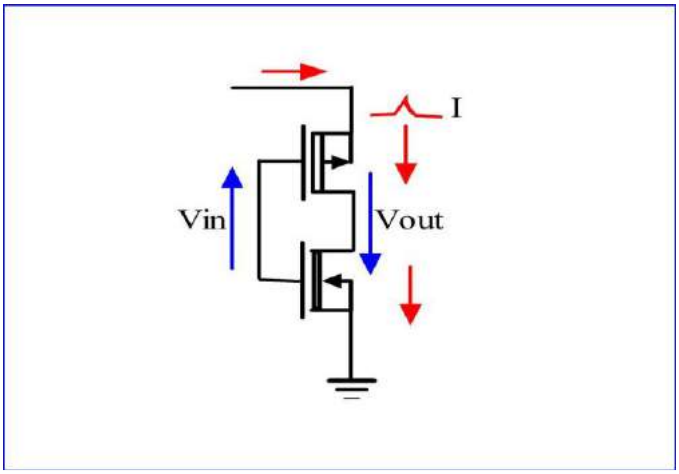
Figure 13 shows the total CC-100IP dynamic reservoir and effective capacitance increases that are the result of the load current impulses imposed on the system supply grid and the CC-100 IP. The **grey** curve is the combination of the dynamic reservoir and effective capacitance, or total capacitance that the CC-100 generates in response to high current impulses, the **blue** curve is the dynamic reservoir capacitance alone. As one can see, the dynamic reservoir capacitance magnitude far outweighs the effective capacitance, and the dynamic reservoir capacitance driven by the magnitude of input dynamic current and supply voltage perturbations.

With a 16pF static output or return capacitance used on the CC-100IP, the magnitudes of the reservoir capacitance approach 10nF. This is an order of magnitude increase with respect to the capacitance provided by standard on chip MOS DCAPs. This is a good example of how the CC-100IP can dynamically enhance supply bypassing at the IC level of integration.

So**,** the 2X increase in small signal effective capacitance, the dynamically controlled increases in large signal, reservoir capacitance, the 25% reduction in ESL, and the resulting 20% to 36% drop in overall Dynamic Current and Power Draw, leads to better high frequency (lower ESL) and low frequency (higher Effective and Reservoir Capacitance-- leading to better filtering capability) filtering (broader dynamic range), and an up to 20% reduction in dynamic power draw. These characteristics lead to lower RF emissions from power grids, cleaner internal chip supplies, smaller DCAP footprints(if filtering area is a concern) lower chip dynamic power dissipation(lower thermal footprint), and greater circuit capacity.

RF EMISSIONS & WASTED ENERGY in Integrated Circuits-The Root Cause

Much energy is wasted in IC chip design, a portion of this waste radiating into free space. In the attempt to keep digital supply lines clean from the noise effects created by high frequency surges of overlap current in CMOS based logic, IC decoupling/reservoir capacitors are used to shunt this current to ground, thus keeping on-chip supplies clean. This current is generally ignored by chip designers, and is treated as “throw away” or ignored current and energy. Unless on-chip supplies are corrupted beyond a 50mV limit, this current is discarded and ignored.



Overlap current will not be ignored, however. Not only is it the source on dynamic power dissipation in chip designs, it shows up spectrally, radiating into space from power grids in ICs, giving away important system information, allowing hackers to gain access and compromise data.

CMOS logic based overlap current flow is the primary source of dynamic power dissipation in digital and mixed signal ICs. If even a small portion of this current can be recovered and reused, chip power dissipation is reduced and data is made more secure.

Figures 14 through 18 are various examples of CC-100IP RF Emission and dynamic power reduction on various processes and circuit architectures.

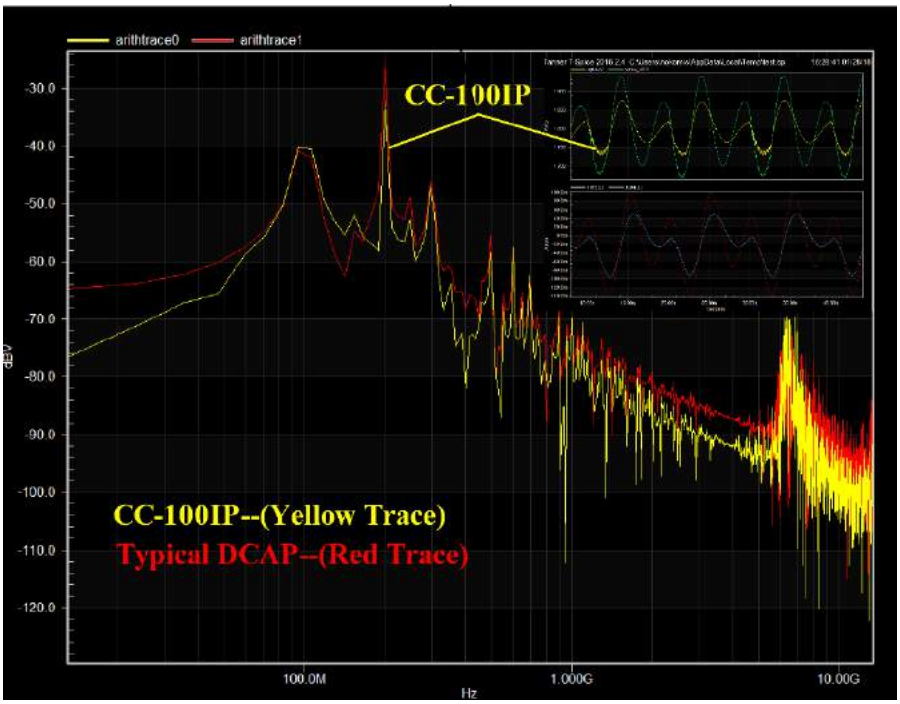


Figure 14: CC-100IP Hyper DCAP Noise Magnitude Reduction (Manufacturing Process: Jazz Semiconductor CA18)

The plot in Figure 14 features not only a drop in overall emissions (the **yellow** curve in Figure 11), but also a 6dB drop in radiated emissions at 200Mhz, which translates to a 75% attenuation of power grid radiated energies(a quarter power point).

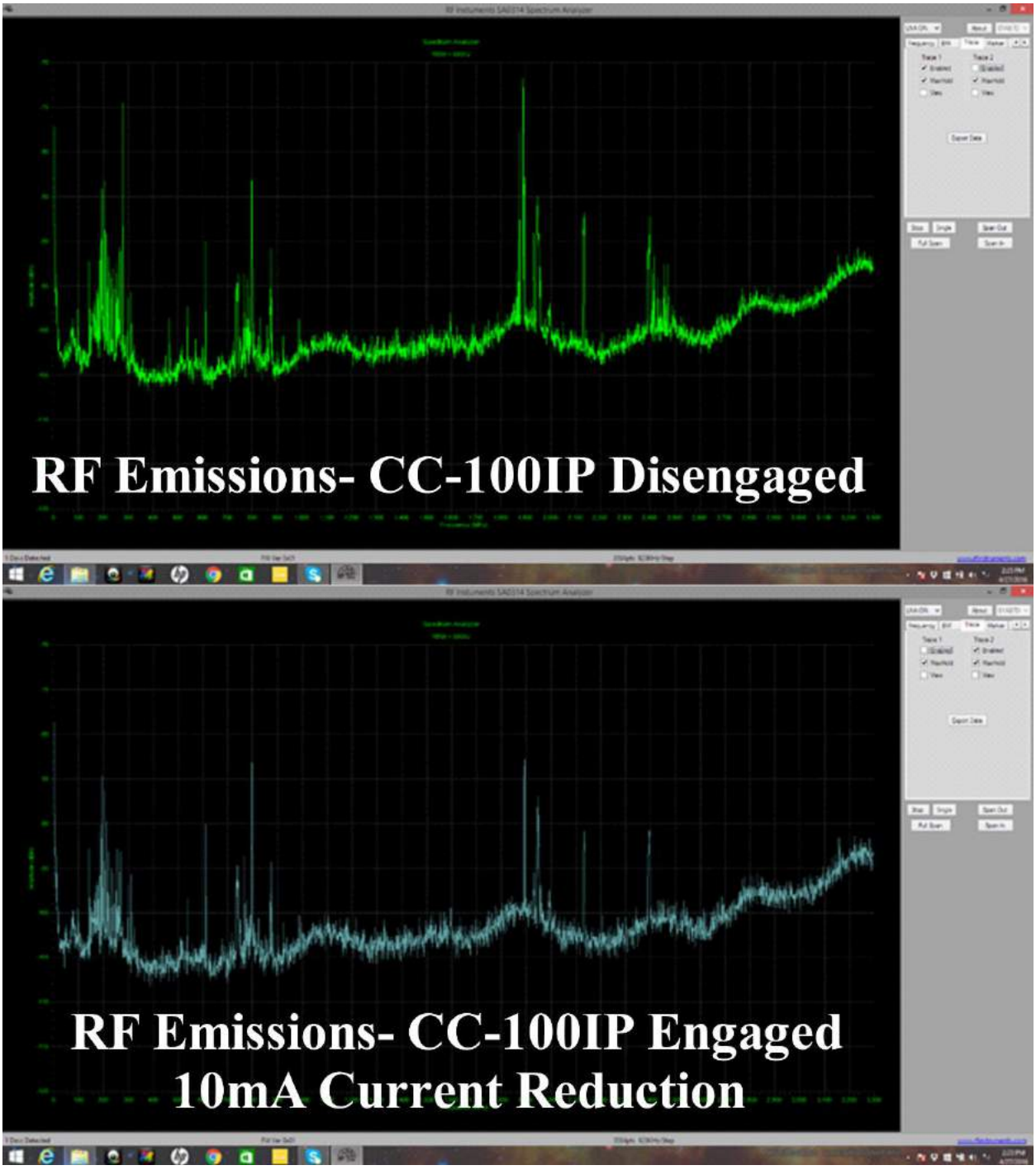


Figure 15: CC-100IP Embedded in a Server Ethernet Controller (prototype)

The Figure 15 plot also shows an overall drop in radiated emissions due to CC-100IP feedback, featuring a 12 dB drop (a 16X reduction) in radiated emissions at ~1.9Ghz. The overall current saved from this reduction in dynamic current is ~10mA.

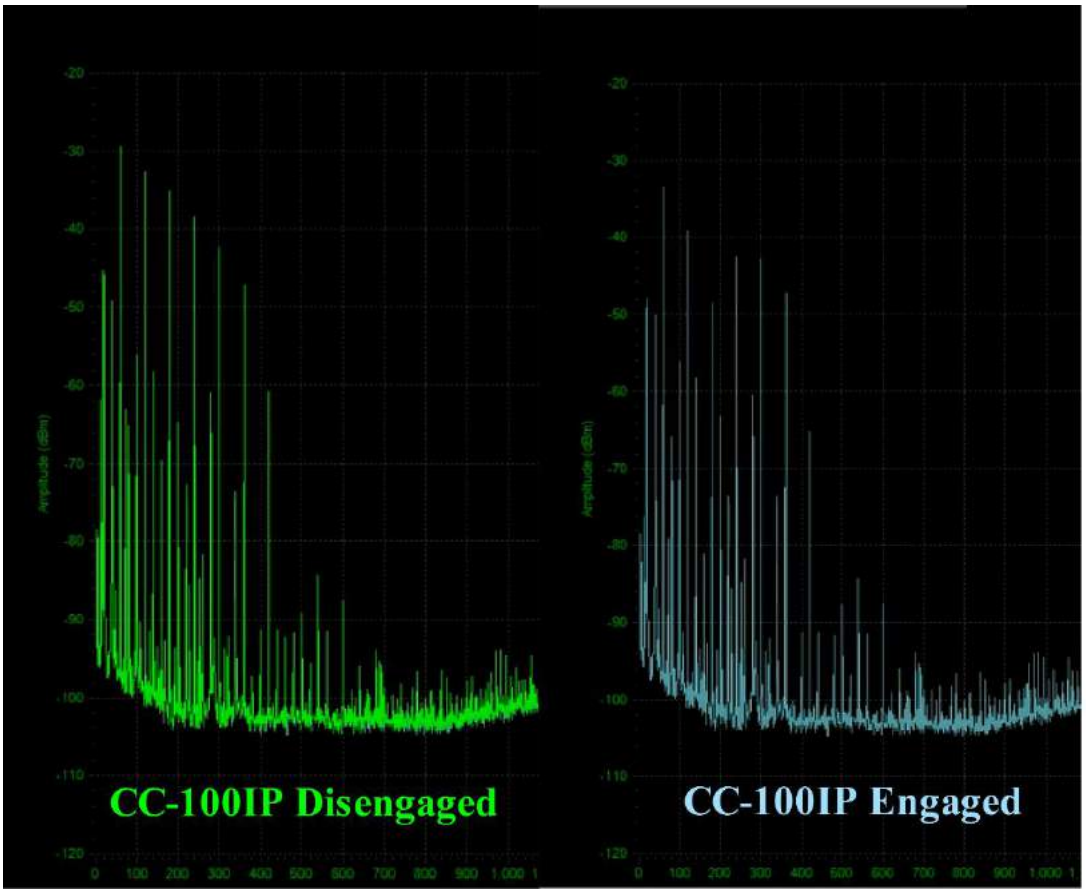


Figure 16: CC-100IP Test Chip Results-20% Current Reduction (Manufacturing Process: GF_018RF)

Figure 16 shows a 6 dB (half power point) broadband RF Emission reduction in a square wave spectrum measured on the CC-100IP test chip power grid. A 20% dynamic current reduction was seen as the result of the emission reduction.

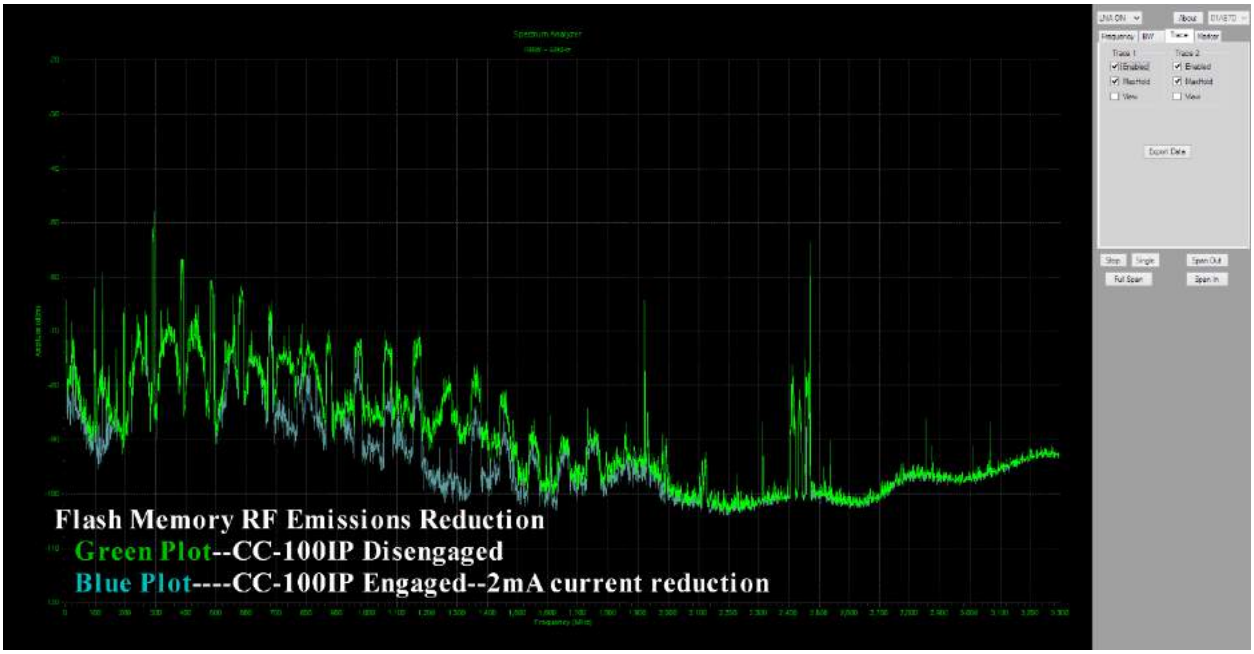
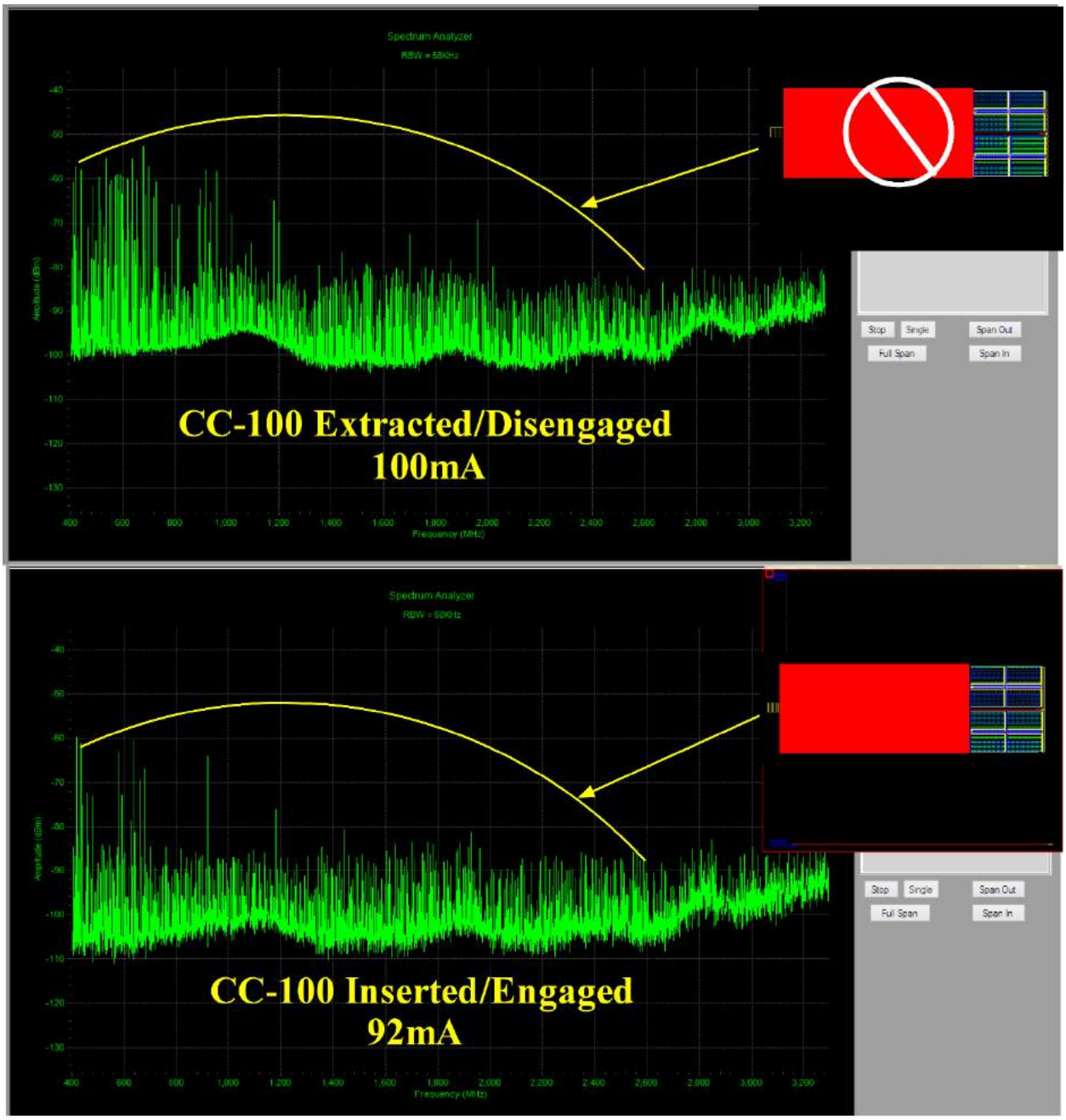


Figure 17: CC-100IP embedded in Flash Memory

Figure 17 shows the disengaged/engaged RF emission spectrums that are the result of the CC-100IP embedded in a flash memory power grid. A 2mA dynamic current reduction is seen as the result of CC-100IP activity.



Missing/Suppressed Frequencies Above
Equals Cancelled Emissions and Current Saved

Figure 18: CC-100IP embedded in a Pseudo Random Generator Test IC (Manufacturing Process: GF_018RF)

Figure 18 demonstrates an 8 mA dynamic current reduction that is the result of CC-100IP RF Emission reduction as a consequence of CC-100IP activity on the power grid of a pseudo random test generator produced by CurrentRF. The pseudo random test generator chip was designed to not only test the CC-100IP, but demonstrate the ability of the IP to be integrated into larger digital circuits.

Power Integrity

CC-100IP EMI Suppression and Power Integrity Enhancement

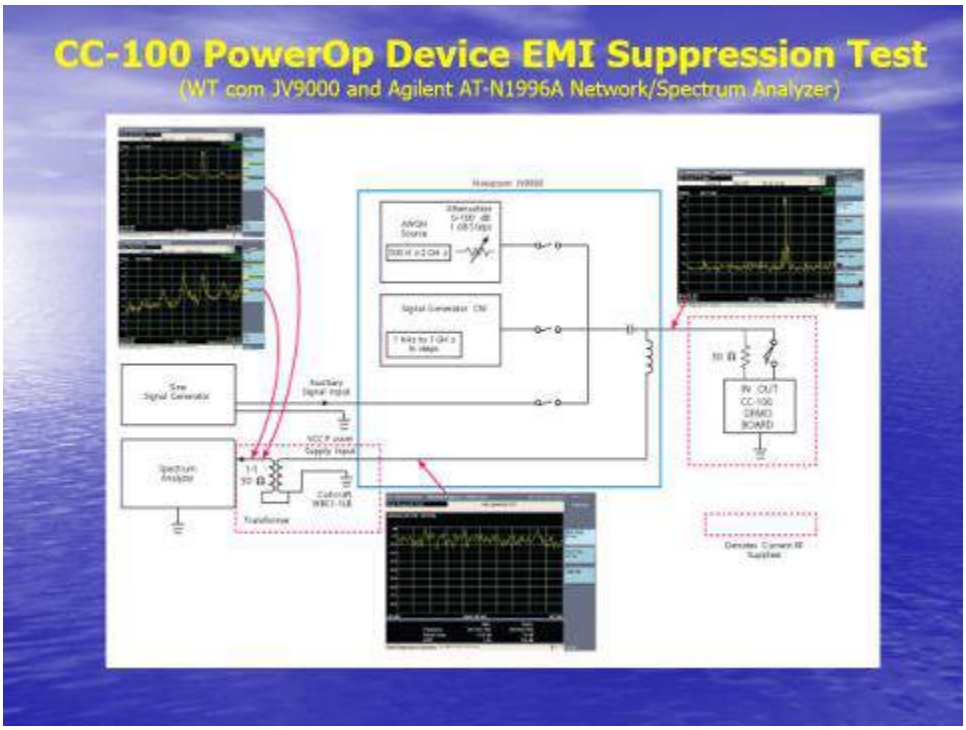


Figure 19: CC-100IP EMI Suppression and Power Grid Compensation Test Set-Up

Figure 19 shows the Wireless Telecom Group (WTcom) JV9000 utilized as an EMI and Power Grid compensation test platform for the CC-100IP. In the Figure 19 device characterization set-up, the DC supply port is utilized as a signal monitor port, outputting the results of device performance to an impedance matching transformer, the output of which is fed to a spectrum analyzer for analysis. The DC Supply port on the JV9000 was designed for VCC biasing, not for signal monitoring, as the port is not impedance matched (see the S_{11} plot of the DC Supply port in the lower middle of Figure 19) to a 50 Ω environment and attenuates the JV9000 output signal by roughly 30 dB. The impedance mismatch of the 50 Ω input of the WBC1-1LB Coilcraft transformer to the unmatched DC Supply port impedance, creates reflective behavior (see Figure 19) between the output of the JV9000, the input of the device, and the input of the WBC1-1LB transformer. The reflective behavior of the JV9000 DC supply port; however,

provides an excellent frequency domain test for the device's EMI suppression capability and the ability of compensating, in a broadband fashion, power grid impedance mismatches.

In Figure 19, the frequency plot shown at the output of the JV9000 displays the spectral characteristics and frequencies applied to the device. The output signal, terminated into a 50 Ω input of a spectrum analyzer, shows a flat -19 dBm JV9000 maximum injected noise floor, and a +2 dBm injected 600 MHz sine wave tone superimposed in the unit on the JV9000 output. Given the JV9000 spectrum applied to the output disengaged device, the two frequency plots at the end of the DC supply port and Coilcraft transformer shows the impedance mismatched, reflective spectrum fed to the spectrum analyzer, with and without the 600MHz injected tone (upper left corner of Figure 19).

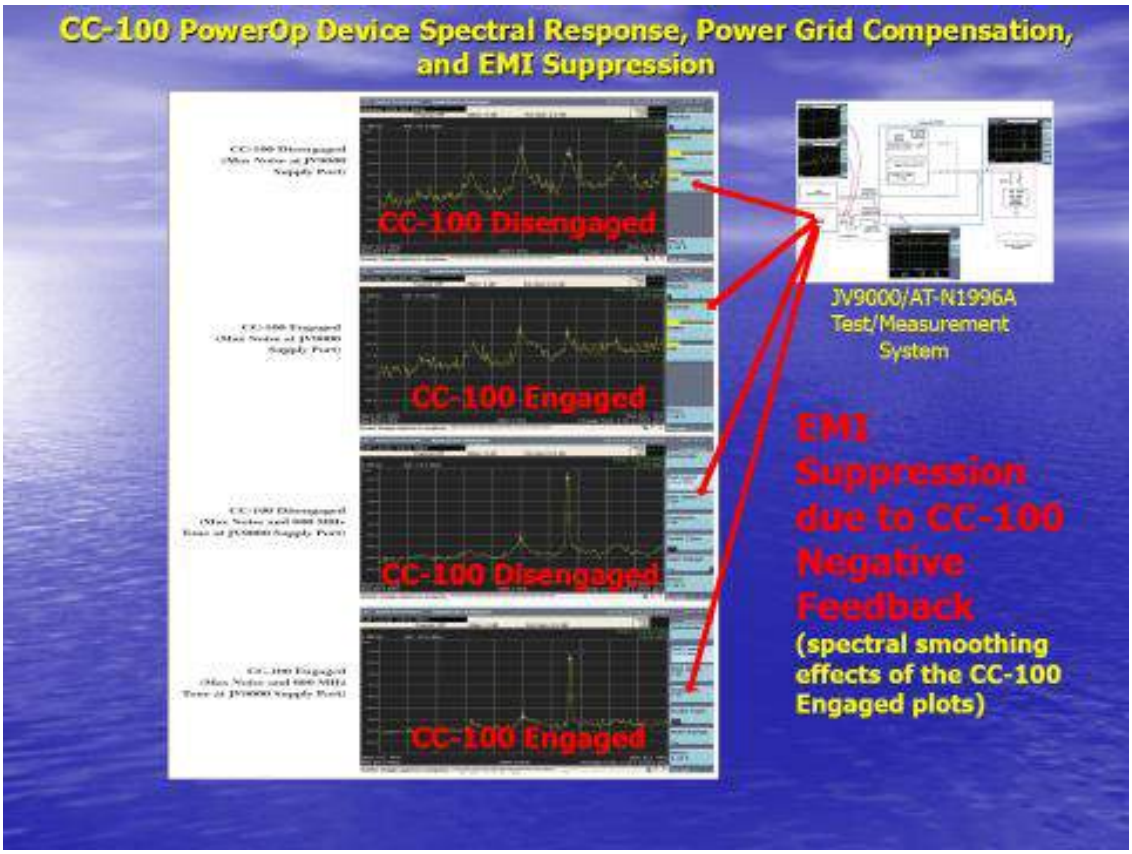


Figure 20: CC-100IP EMI Suppression and Power Grid Compensation

CC-100IP Compensation Performance

Figure 20 shows the spectral results of the Power Optimizer with and without the CC-100 device's output engaged in the Figure 19 test system. The plots on the left show the spectrum seen at the spectrum analyzer input with the device engaged and disengaged. Peaking and reflection in the spectrum is observed, with major peaks in the noise only spectrum at 400 and 600 MHz at approximately -51 dBm levels, and the injected 600 MHz tone applied to the device at a -24 dBm level. The plots in Figure 20 with the device engaged, show reduced spectral peaking and reflection, the major peaks at 400 and 600 MHz at approximately -54 dBm, and the injected 600 MHz tone applied to the device reduced to -28 dBm.

Thus, a 3 to 4 dB reduction (half power point) in spectral reflection and peaking is shown in the device, JV9000 driven tests, yielding a smoother, flatter spectrum, with the device compensating for system termination mismatches and consequent signal reflection on impedance mismatched nodes. The JV9000 tests correlate well to the S_{11} measurements taken and displayed in Figures 5 and 6, showing the Power Optimizer capability in compensating for system and power grid mismatches.

CC-100IP Behavioral Model

To facilitate easy integration of the CC-100IP into new designs, CurrentRF has created an easy to use behavioral model that can be dropped into the top level of digital and/or mixed signal design as easily as typical DCAPs are placed into designs to provide on-chip bypassing and reservoir capability.

Figure 21 shows the schematic details of the CC-100IP Behavioral Model. The CC-100IP Behavioral Model is built from Standard Spice components found in any Spice based simulator (Cadence, Mentor Graphics, Silvaco/SmartSpice, etc.). The W0 Switch and GG1 VCCS parameters can be changed for maximum CC-100IP performance and applied to the Figure 22 System Test Bench.

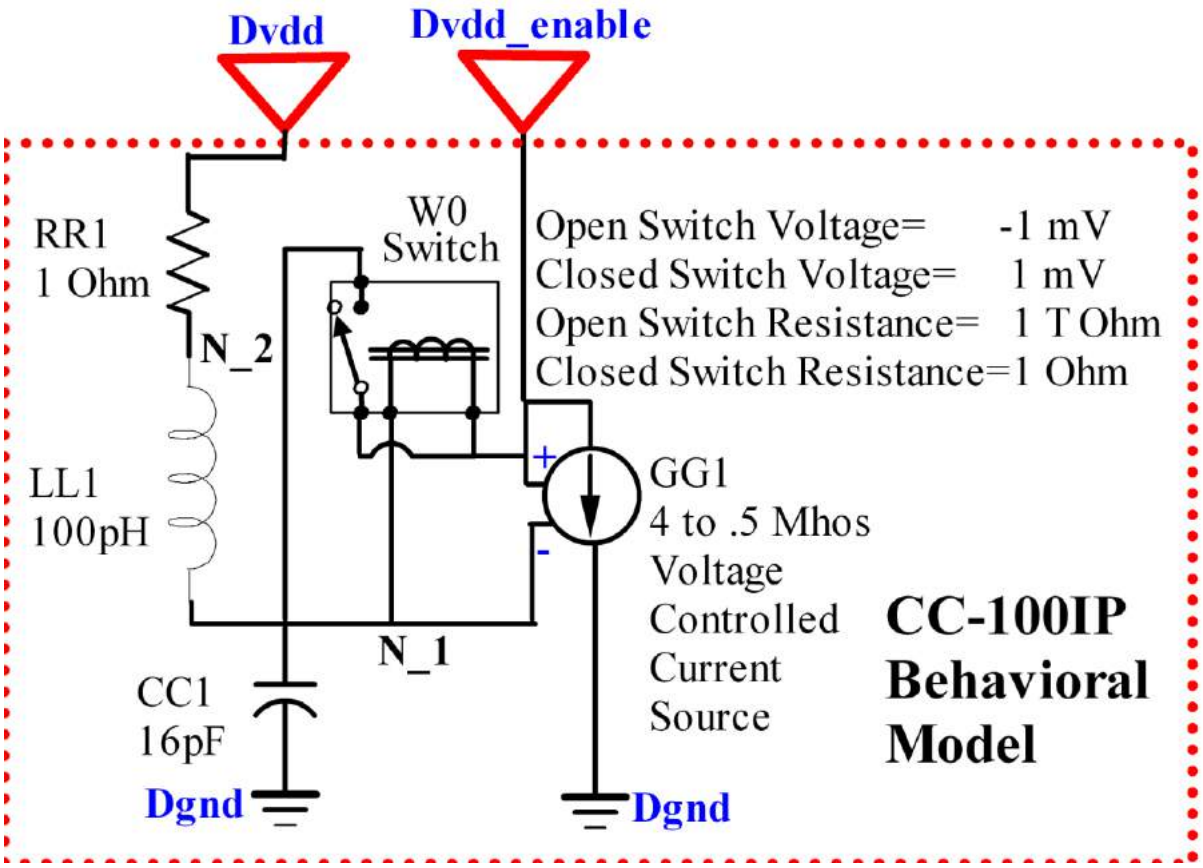


Figure 21: CC-100IP Behavioral Model Schematic

CC-100IP Top Level Test Bench

Figure 22 shows the schematic details of the CC_100IP top level evaluation test bench. The stimulus logic circuit can be anything that contains active CMOS logic. CurrentRF has used simple, clock driven inverter chains and more complex logic (adders, exor gates, etc.) to test the actual IP and it's behavioral model. Contact CurrentRF for additional details.

The W0 Switch and GG1 VCCS parameters can be changed for maximum CC-100IP performance and applied to the Figure 22 System Test Bench. These final parameters should be communicated to CurrentRF, as they will guide the structure of the finial Silicon IP design.

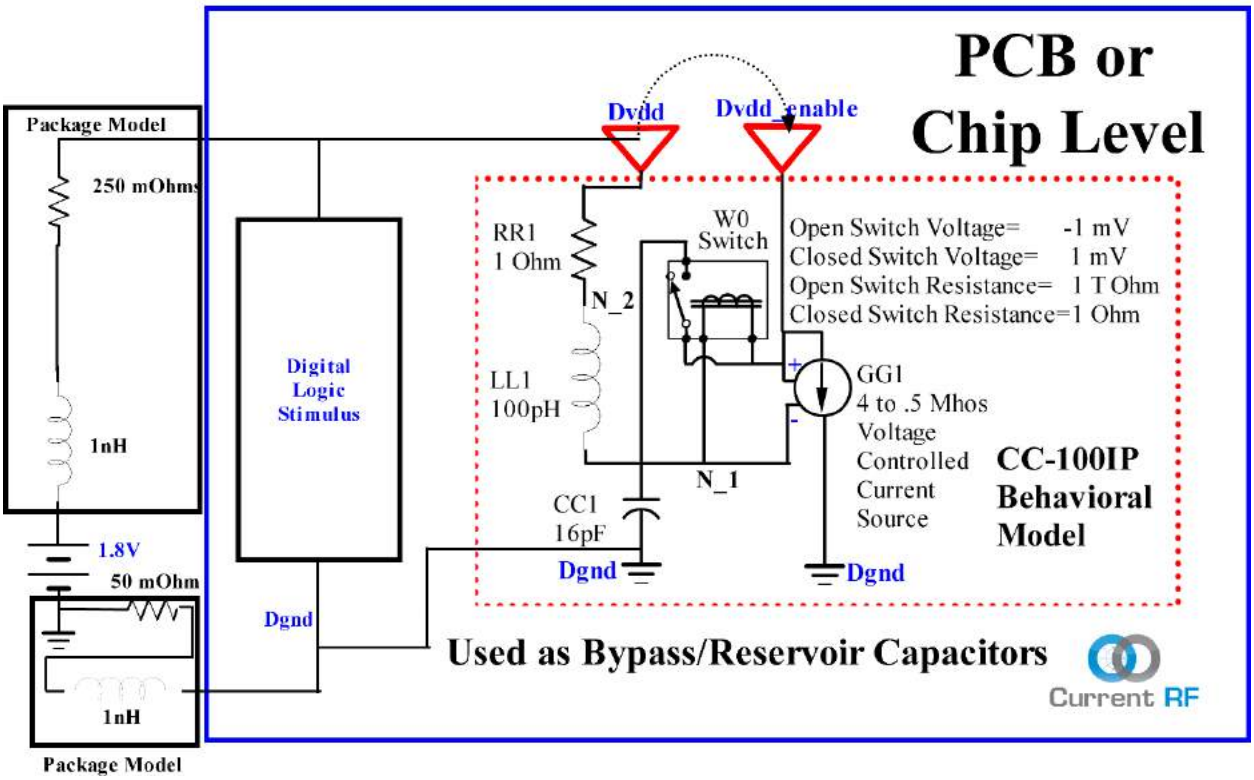
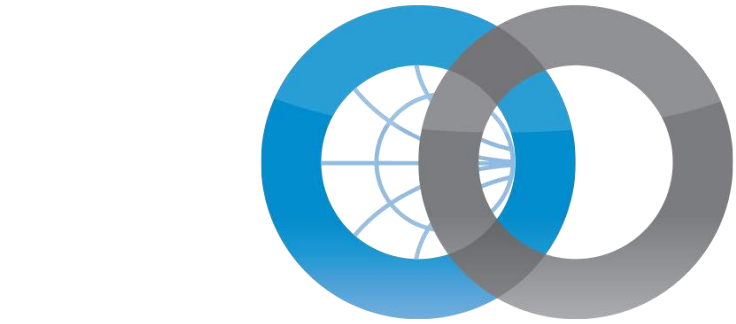


Figure 22: CC-100IP Behavioral Model Schematic and Top Level Circuit and Stimulus

Based on Simulation results with the behavioral model shown in Figures 21 and 22, the CC-100 IP can be customized for any application and process node. Contact CurrentRF for details.

For additional technical or ordering information contact us at:



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