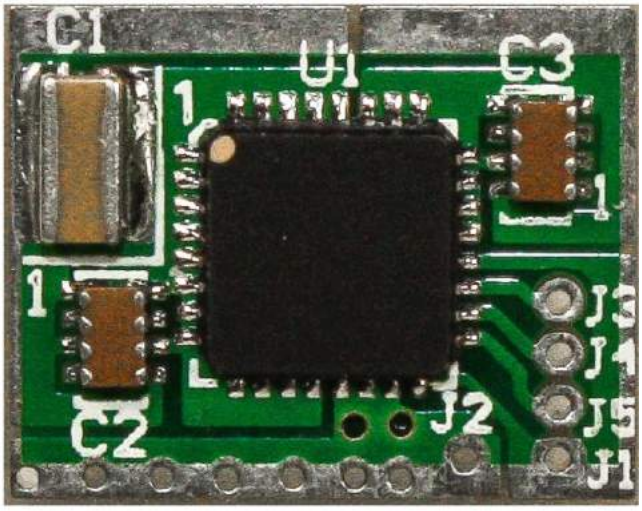
Current RF

CC-100

Power Optimizer

Silicon Super Capacitor



General Description

Electronic systems that use digital signal processing circuits (DSP) generate noise currents as an undesired byproduct of their function. These noise current impulses are too high in frequency for conventional regulators to supply directly, thus bypass capacitors are utilized in conjunction with system voltage regulators to supply these needed high frequency currents. The added bypass capacitors also function to reduce supply voltage noise by bypassing the digitally generated, high frequency noise currents to system ground. This bypassing action shunts the high frequency noise currents away from the supply line, causing a “throw away” power drain on system power sources, batteries, and capacitors.

Power draw due to digitally derived noise currents can be greater than 50% of the total device and system power consumption, and is especially significant in portable devices, such as smart phones and portable computing devices, laptops and Ipads, medical devices, ultra-low power systems powered by low capacity energy harvesting devices, and the like. Digital power drain tends to increase as application complexity increases in computers and smart devices.

The CurrentRF CC-100 Power Optimizer (PowerOp) is designed to intercept “thrown away”, digitally generated, currents and recycle them back into the system. This current recycling can improve system battery life in portable devices by as much as 36%.

Designed to be inserted in series with the ground side of a major system board bypass capacitor, the device has an ultra-low input impedance small enough so as not to interfere with the normal function of a PCB bypass capacitor. The output impedance of the CC-100 is high enough to force, with the inclusion of an appropriately sized return capacitor, “thrown away” currents back into the system.

The CC 100 is available in a 5mm x 5mm 32 lead QFN package, for optimal component size to board layout density applications. The device is characterized for operation from 0C to +85C

Features

Topology

- Ultra-low Input Impedance Design
- Single High Impedance Output
- Uni-Directional Operation
- Proprietary/Patent Pending Topology

Performance

- Low Power Sensitivity
- High Power Handling Capacity
- High Output Impedance
- Ultra-low Input Impedance
- Pico-Second Response Time

Functional Block Diagram

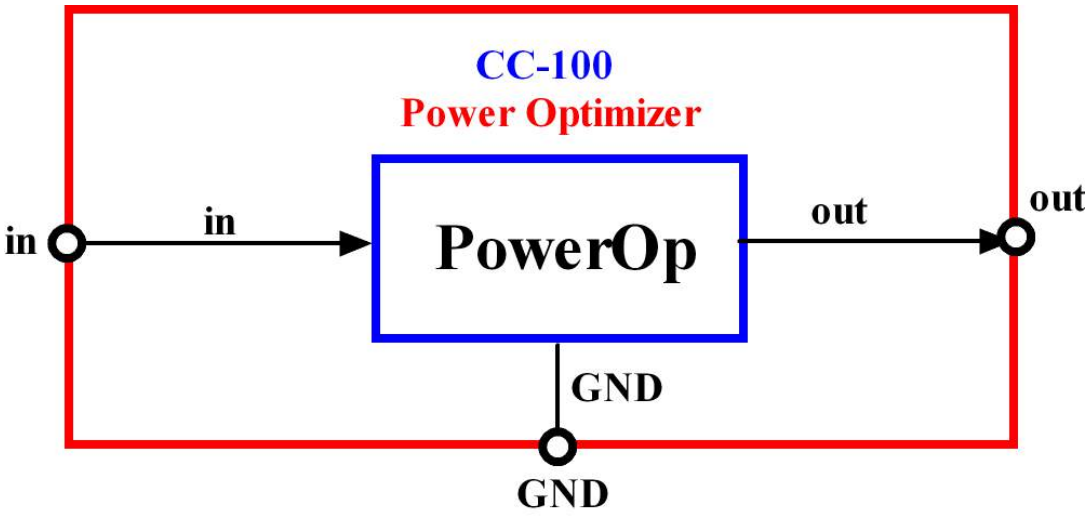


Figure 1: CC-100 Block Diagram

Figure 1 above shows the internal block diagram of the CurrentRF CC-100 Power Optimizer. The CC-100 is a three terminal device designed to harvest “throw away” current generated as the result digital switching activity or an impressed AC noise current source.

The CC-100 has no system supply or power overhead requirement for operation, and needs only a single, system ground for device operation.

Designed to be inserted in series with the ground side of a major system board bypass capacitor, the device has an ultra-low input impedance small enough so as not to interfere with the normal function of a PCB bypass capacitor, and an output impedance high enough to force, with the inclusion of an appropriately sized return capacitor, “thrown away” currents back into the system.

Pinning Information

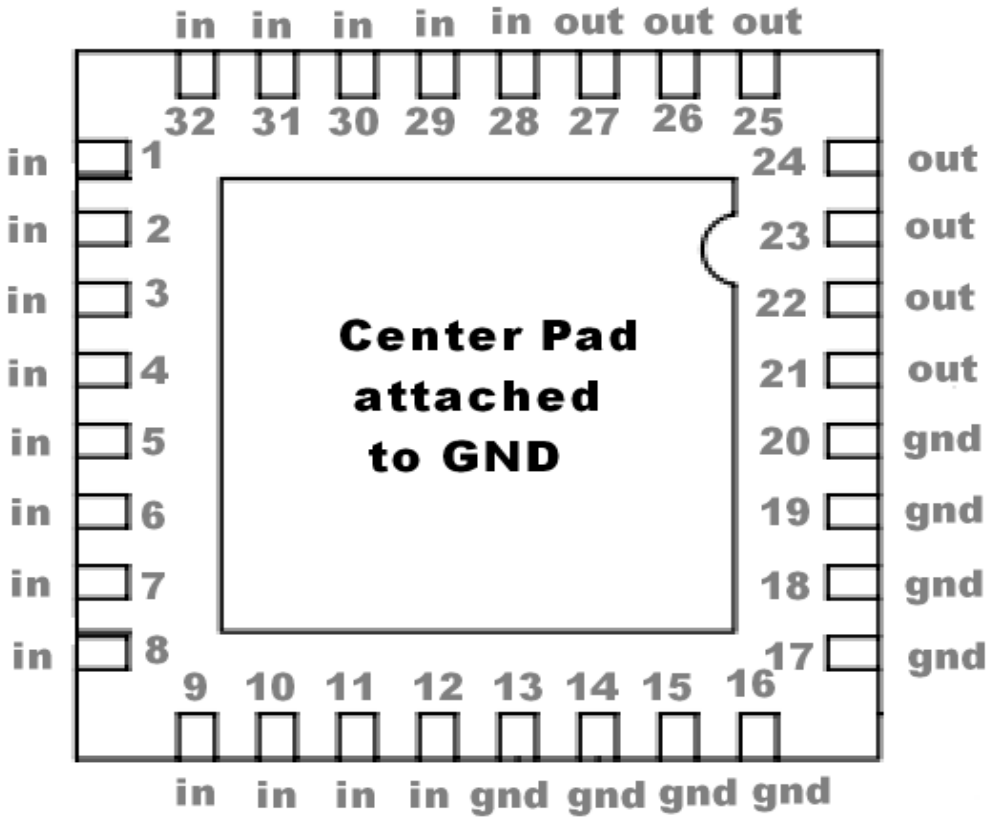


Figure 2: Package Pin Out

Symbol	Pin	Type	Description
in	**1-12;28-32**	**Input**	**low impedance input**
out	**21-27**	**Output**	**current output**
GND	**center pad,13-20**	**ground**	**ground connection**

Table 1: Pin Descriptions

Functional Description

The CurrentRF CC-100 Power Optimizer (PowerOp) is designed to intercept digitally generated, “throw away” noise currents and recycle them back into the system, thus improving system battery life in portable devices by as much as 36%.

The CC-100 harvests “throw away” current, the device being inserted, unobtrusively, in series with the ground side of a major system board bypass capacitor. With all CC-100 inputs tied to the ground side of a system bypass capacitor, the device input’s profile a state-of-the-art, minimal input impedance, enabling wide bandwidth currents to be recovered and returned to the system. Due to the input parallelism, the user can adjust the CC-100 input impedance to be low enough so as not to interfere with the normal function of a PCB bypass capacitor. The user can also tailor the device input impedance(disconnecting device inputs) for optimizing system supply line noise and maximum current recovery.

The CC-100 output impedance is set high enough to force, with the inclusion of an appropriately sized return capacitor, “thrown away” currents into a selected system supply.

Limiting Values

Symbol	Parameter	Conditions	min	typical	max	unit
Vin	max input voltage	without bypass cap input(no AC coupling)	-0.3		2	**V**
Vout	max common mode voltage	without return cap input(no AC coupling)	-0.3		2	**V**
Imax	Maximum I/O current	RMS AC			10	**A**
Tamb	case temperature	For operation within specification	-40		85	**C**
Vesd	Electrostatic discharge voltage	HBM		2000		**V**
		CDM		500		**V**

Table 2: Limiting Value

Recommended Operating Conditions

Symbol	Parameter	Conditions	min	typical	max	unit
Vin	max input voltage	without bypass cap input(no AC coupling)	-0.3		0.3	**V**
Vout	max common mode voltage	without return cap input(no AC coupling)	-0.3		0.3	**V**
Imax	Maximum I/O current	RMS AC			1000	**mA**
Tamb	case temperature	for operation within specification	-40		85	**C**

Table 3: Operating Condition

Dynamic Characteristics

Introduction

The CC_100 PO/SSC IC is the basis of a power saving and sensitivity enhancement sub-system that shows advantage if implemented in any system containing digital processing and switching events. The sub-system is simple, consisting of the CC_100 PO/SSC reference design, scattered at strategic positions throughout a given system. The power savings with the system in place, ranges from over 35% (surge conditions) to 3%(worst case), and is highly dependent on the slew rate and surge current of given logic and system transitions.

Due the dynamic noise cancellation inherent in the sub-system, the RF/analog sensitivity has been shown to increase with the inclusion of the sub-system from -143dBm to -146 dBm, and spectral characterization has shown significant supply line noise reduction from 500Mhz to 3 Ghz. The CC_100 PO/SSC IC can also aid in classical noise reduction in RF and Analog system front ends.
The CC_100 PO/SSC has been fully tested and characterized, and represents a significant breakthrough in dynamic power and dynamic noise reduction. The IC is in production and is readily available from CurrentRF.

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All electronic systems that use CMOS digital circuits generate EM noise and currents as an undesired byproduct of their function, as shown in **Figure 3**. These EM noise and current impulses are too high in frequency for conventional regulators to supply directly, thus bypass capacitors are utilized in conjunction with system voltage regulators to supply these locally needed high frequency currents.

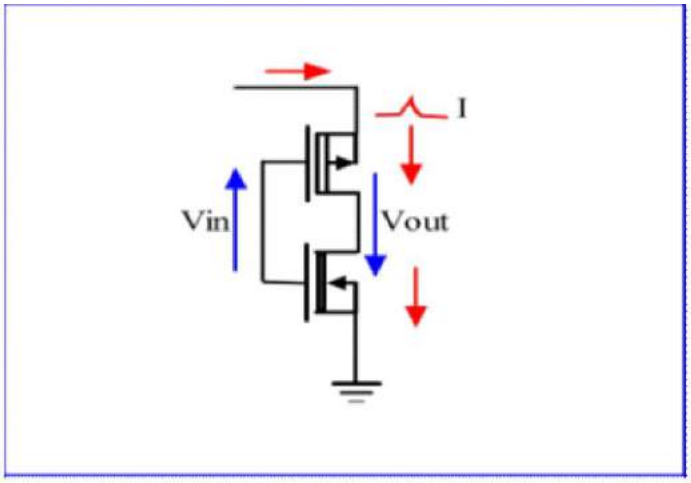


Figure 1: CMOS Inverter Example

The added bypass capacitors function to provide a local high frequency current reservoir for local logic, reducing supply EM noise by bypassing the digitally generated, high frequency noise currents to system ground. This bypassing action shunts the high frequency EM surges and noise currents away from the supply line, as shown in **Figure 4**, ultimately causing a "throw away" DC power drain (i.e. DC recharging of the bypass capacitors due to the losses in the system) on system power sources, batteries, and capacitors. 4

Figure 4 shows typical reservoir current flowing (the "red" waveform) as the result of active digital circuit surges and a typical system bypass cap (C4). Current spikes up to 1 A are shown. The "integrated circuit" in the figure can be any IC in any system that has some amount of digital activity on board (the circuit in **Figure 3**, as an example). Power draw due to these digitally derived noise currents and losses can be greater than 50% of the total device and system power consumption. They are especially significant in battery operated systems and portable devices, such as smart phones, portable computing devices, laptops and iPads, medical devices, ultra-low power systems powered by low capacity energy harvesting devices, and the like. This form of digital power drain tends to increase system size weight and Power

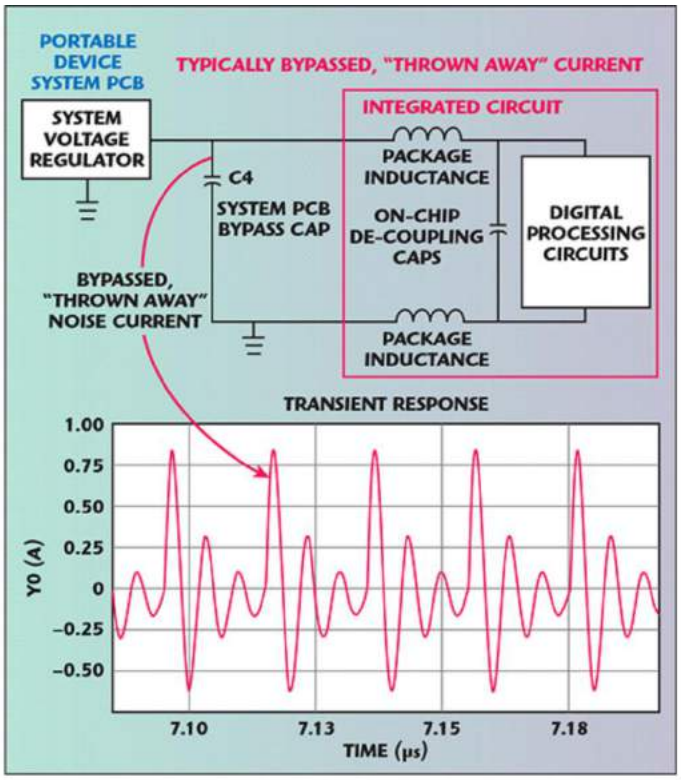


Figure 2: Typical Wasted Energy Scenario

(SWaP) as the consuming device is utilized more heavily and application complexity increases in digitally driven systems.
To reduce the above mentioned EM power drain, the conventional design wisdom is to use digital strategies in design so as to periodically deactivate power hungry digital circuits (some form of “burst mode” processing), minimize digital supply voltages, or “process shrink” the design to a lower gate length manufacturing process node. The strategies above can be thought of as power saving “defensive” actions, the designer striving to reduce switching circuit power drain as much as possible. Utilizing the above strategies generally requires some form of design rework on the digital circuits in order to accomplish the desired power reduction, which adds to time to market and cost. It should be noted, that no matter what “defensive” choices designers make in attempting to reduce digital EM power drain, a certain magnitude of “thrown away” current and power always remains when switching circuits are active. So long as designers use electron-based transistor devices in design, this type of energy waste will be present. This form of power drain can be thought of as a previously “forgotten” EM energy source embedded in switching systems, considered unreachable and unusable, until now.
A methodology and a design has been developed that can reduce the aforementioned digital power drain, tapping into this “hidden” source of wasted power, without the need for costly digital design rework. The methodology and design is intended to be a “supplement” to existing digital and system designs, at the IC, PCB and system levels of integration. Targeting digital “thrown away” currents, the methodology and design intercepts and recycles these currents back into a given system. The implementation on the methodology is small and inexpensive enough to be integrated into existing ICs, PCBs, and systems, drawing no operational power of it’s own.
5

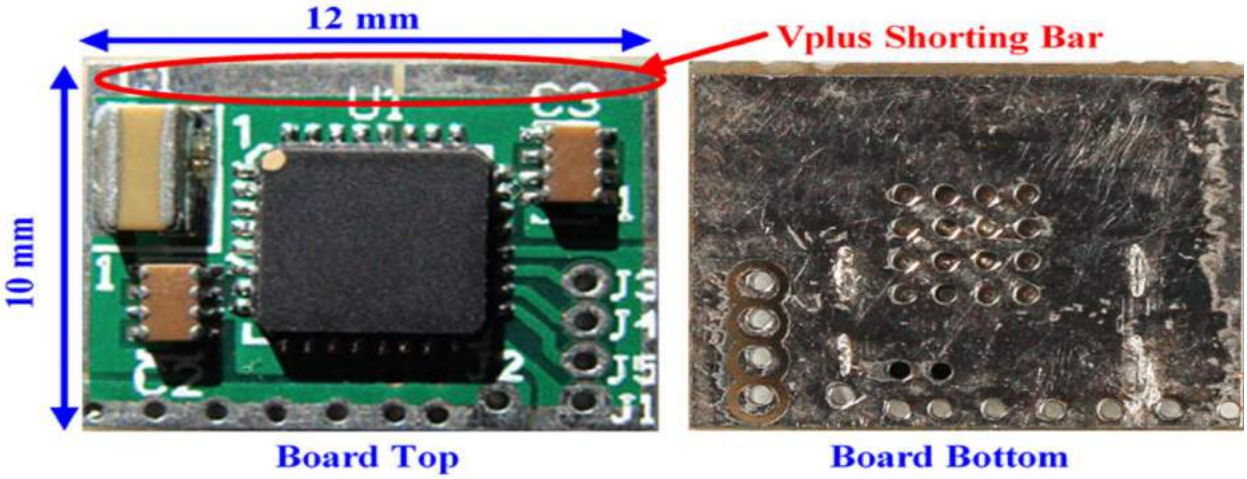


Figure 3: CC_100 PO/SSC IC and Reference Design

1.1 Existing CC_100 PO/SSC Monolithic IC and USB Packaging

The CC_100 Power Optimizer IC (PowerOp)/Silicon Super Capacitor (PO/SSC) and reference design is shown in **Figure 5**. This existing 48 lead, RF IC, manufactured in 2013 on what was then the IBM CMRF7SF manufacturing process (now Global Foundries) can be inserted into any existing design, essentially replacing the system supply line bypass capacitors inserted to create and maintain system supply cleanliness. The CC_100 Power Optimizer IC (PowerOp)/Silicon Super Capacitor (PO/SSC) and

reference design has been manufactured and tested, and fits easily in any system footprint. Given that the CC_100 exists, is an RFIC, has been tested, characterized, and sold in various venues and to various customers, it is the perfect candidate for the reduction of size, weight, and power (SWaP) in CubeSat satellite systems.

This device, inserted in series with the ground side of a major system board bypass capacitor(s)(C1 and C2 in the Figure 5 reference design), has an ultra-low input impedance small enough so as not to interfere with the normal function of a PCB bypass capacitor. The output impedance of the device is high enough to force, with the inclusion of an appropriately sized return capacitor (C3 in the Figure 5 reference design), “thrown away” currents back into the system.

The CC_100 PO/SSC applications reference design PCB, shown in Figure 5, is a 2 layer board designed for ease of evaluation in customer systems. The base board was designed to simply replace an extracted and removed system bypass capacitor for the purpose of system dynamic power reduction. The top of the board in Figure 5 contains the CC_100, routing, and all capacitors needed for PO/SSC IC operation. The bottom of the board is the evaluation board ground plane (no solder mask) and is designed to be soldered directly onto the system ground plane for optimum grounding and AC operation.

To use the CC_100 PO/SSC applications reference design, remove a major system bypass cap or caps, solder the reference design onto the system ground plane, then connect the targeted supply to the applications reference design Vplus Shorting Bar(shown in Figure 5) at the top of the board. If the system bypass capacitors on the targeted supply are of a low quality factor(Q) (Electrolytic, Tantalum, etc. High ESL and ESR), the system bypass capacitors may remain installed.

1.2 Typical CC_100 PO/SSC IC PCB Integration

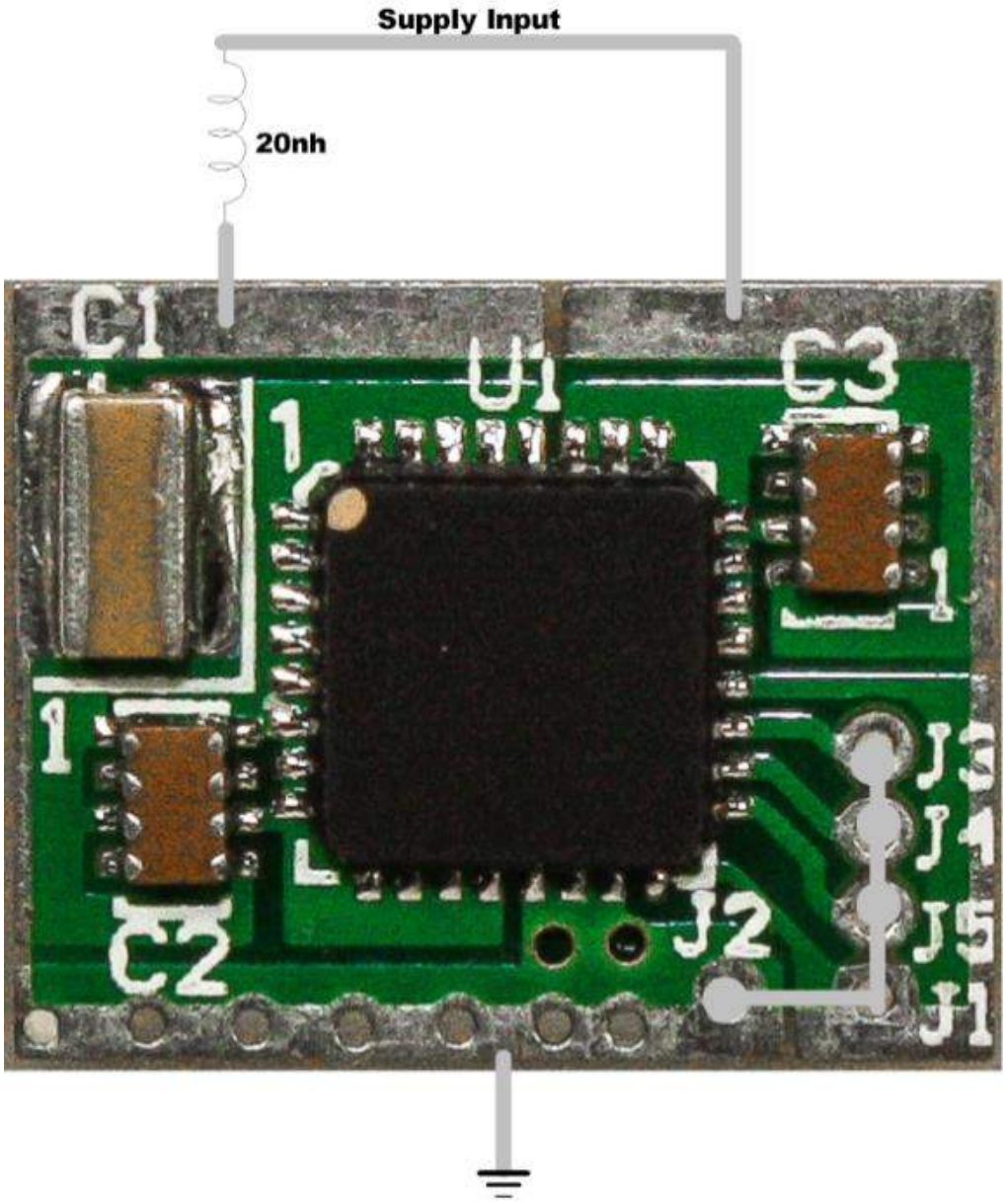


Figure 6: Low Transition Slew Rate Operation Circuit

The CC_100 PO/SSC IC recycles energy on logic transitions with high slew rate edges. The device is totally dependent on the quality, edge transition slew rate, and the speed of the logic and switching circuits from which it harvests and recycles energy.

Typically, a simple power supply connection to both sides of the Vplus Shorting Bar, shown in Figure 5, is all that is needed for PO/SSC IC operation.

In some cases, however, theCC_100 PO/SSC IC encounters logic and switching systems that possess edge transition slew rates that are lower than 5ns(very slow by

today's standards), causing the CC_100 IC to operate with lower efficiency. In these cases, it is suggested that a high Q, 20nH inductor, as shown in Figure 6, be inserted in series with the CC-100 IC input to restore proper device efficiency. The same effect can be accomplished by driving fewer input pins on the CC-100 device, thus increasing the device and application circuit's effective input inductance.

1.3 CC_100 PO/SSC IC Board and Plane Implementation

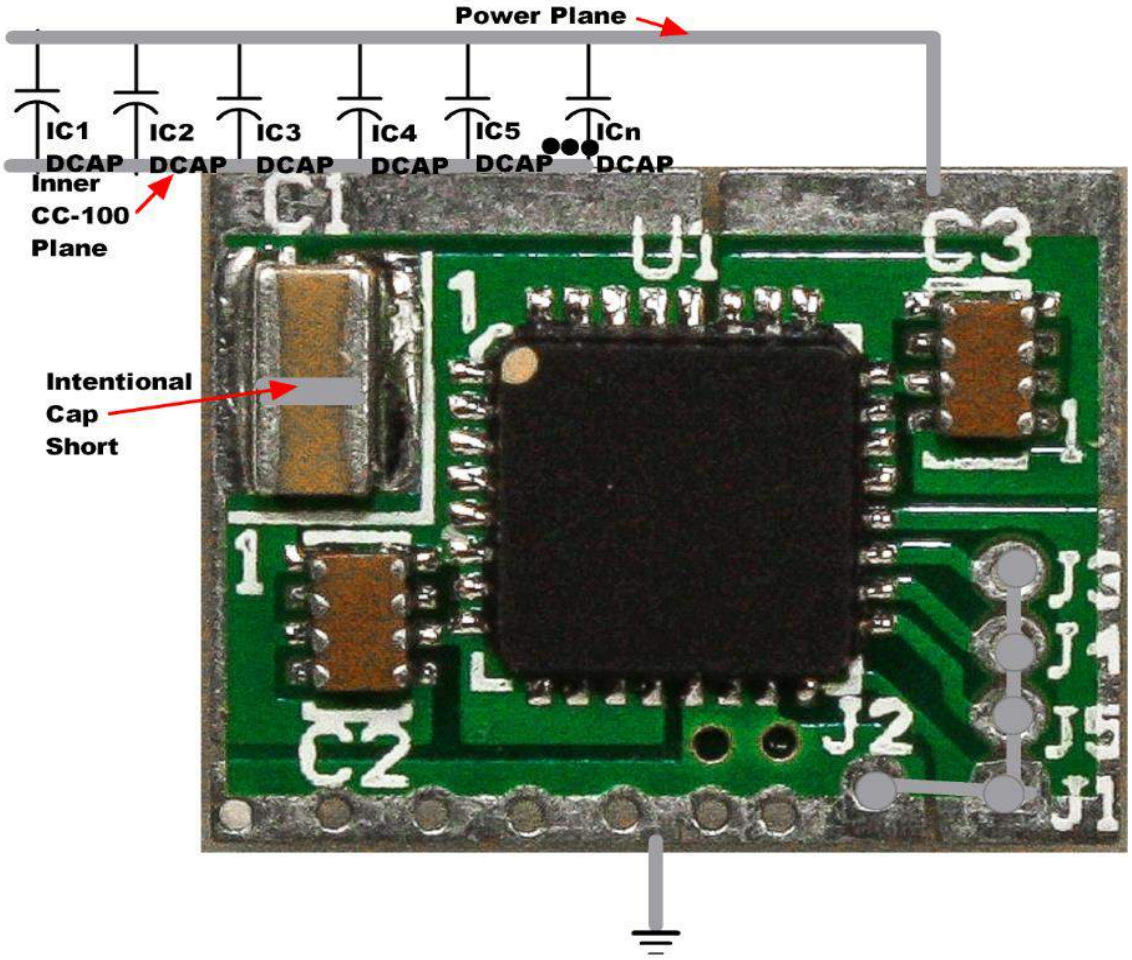


Figure 7: Board and Plane Implementation

More waste system energy may be captured and recycled by the CC_100 IC if all system logic bypass caps are connected to a dedicated internal CC_100 PCB plane as shown in Figure 7. The caps in Figure 7 bridge the system power plane and the internal CC_100 plane, creating a board level, composite input coupling capacitor for the CC_100 IC. To implement this application, simply short the C1 input cap on the CC_100 PO/SSC IC reference design and directly connect the board CC_100 internal plane to the input of the PO/SSC board, as shown in Figure 7. The internal CC-100 plane needs

to be wide and of extremely low inductance, so as not to present an impedance to the system board supply bypassing function. The output of the PO/SSC board is hard connected to the system power plane, as in the applications shown in Figures 6 and 7.

1.4 Characterization Data, Structures, and Test System for the CC_100 PO/SSC Monolithic IC and Reference Design, Including PowerStic-Exodus Packaging

The CC_100 PO/SSC IC has been tested in the applications reference design configuration (see the inserted reference design in Figures 6 and 7).

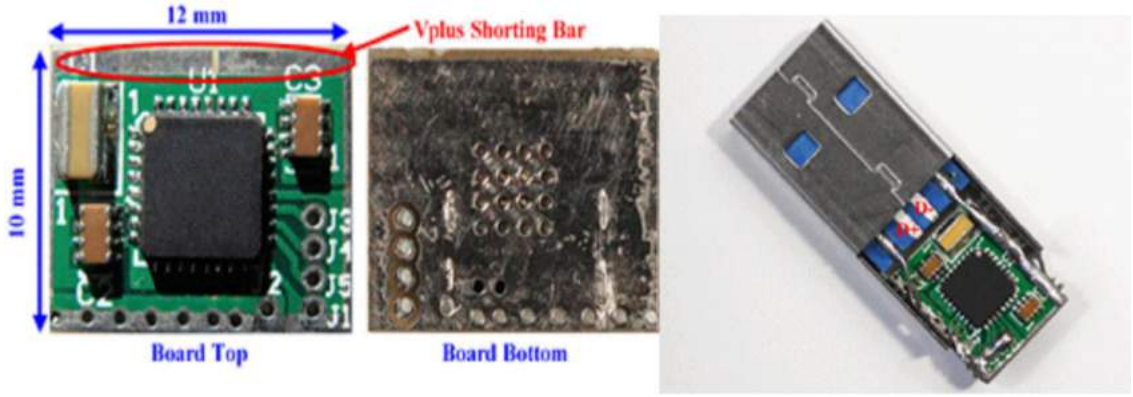


Figure 8: CC_100 PO/SSC IC and Reference Design with USB Packaging

The CC_100 IC has also been tested in USB Powerstic and Exodus configurations shown in Figures 8 through 12. The USB packaged PowerStic and Exodus devices were proven to be electrically “transparent” with respect to the CC_100 PO/SSC reference design, yielding no discernable differences in CC_100 PO/SSC IC performance, regardless of the packaging configuration.

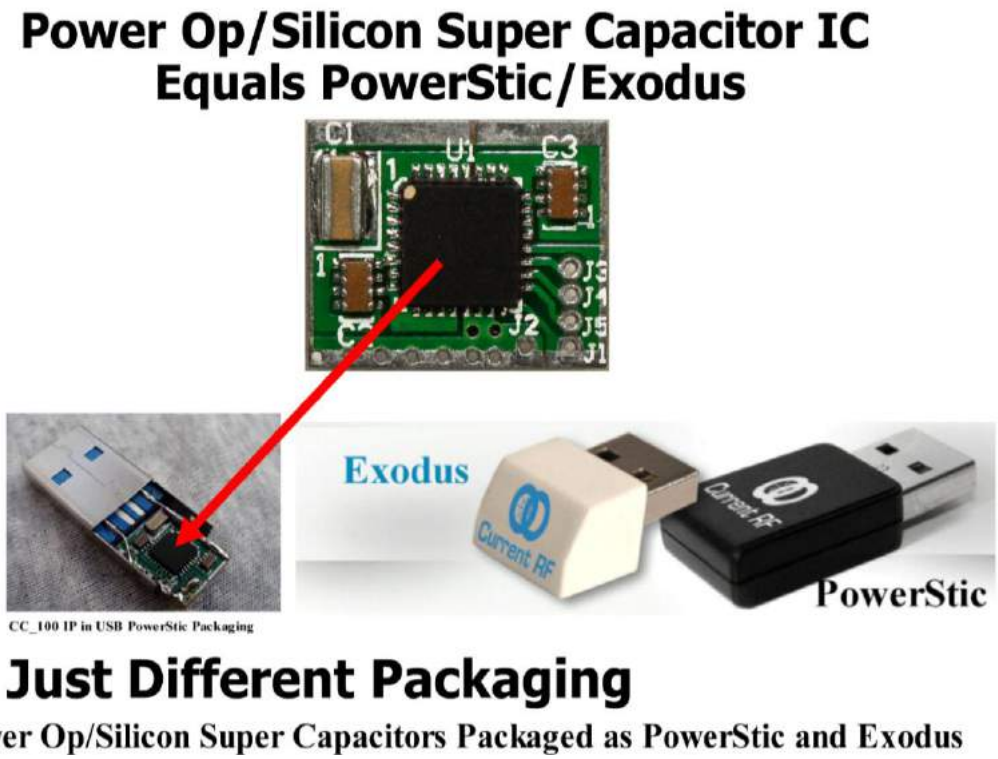


Figure 9: CC_100 PO/SSC IC Driving PowerStic and Exodus Products

As shown in Figures 8 and 9, the CC_100 PO/SSC applications reference design PCB fits in the USB housing selected for the PowerStic and Exodus packaging.

As seen in Figures 8 and 9, the CC_100 and PowerSic-Exodus test and demo board shows the CC_100 PO/SSC IC with various packaging option possibilities for the purposes of easy device testing and demos.

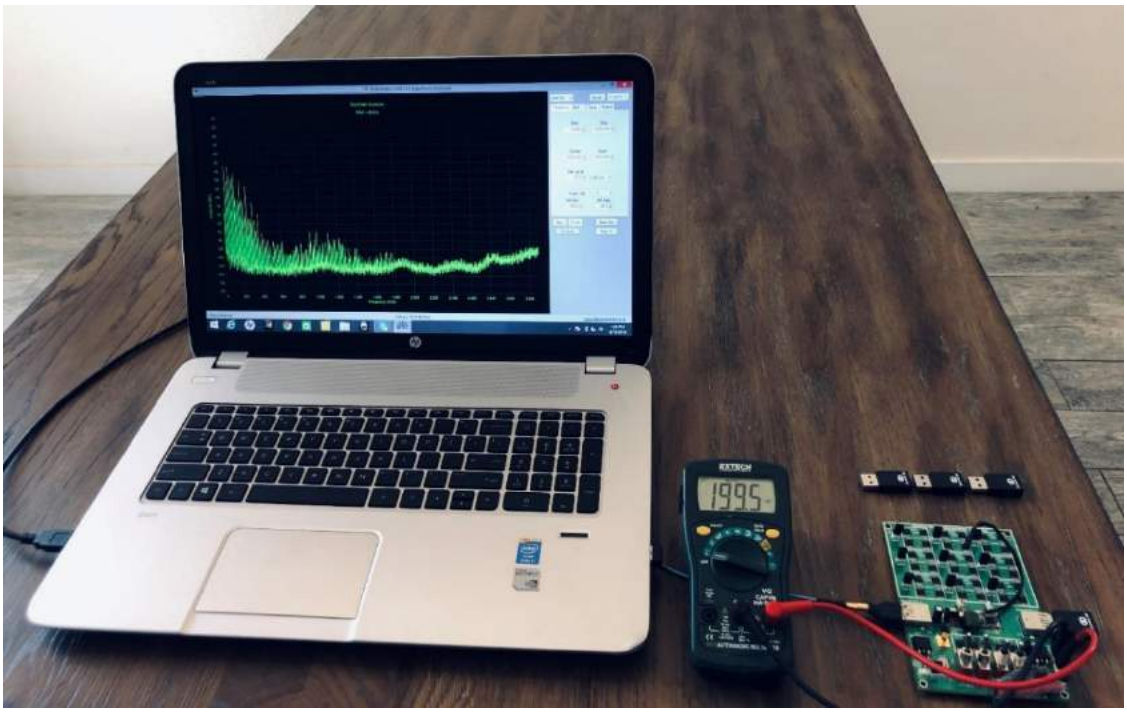


Figure 10: CC_100 PO/SSC IC/PowerStic/Exodus Portable Test System

The Figure 10 test system consists of a reference design and USB test PCB, the PCB including an on-board LFSR for mV level Pseudo-Random supply line dynamic noise generation, 5 parallel connected PLLs for sub-mV dynamic noise generation, clock generation circuits, voltage regulators, and other DUT and test system support circuits. The test PCB includes two USB ports, one for USB DUT insertion and extraction, the other for a supply line monitor feeding a USB powered, PC driven 3 Ghz spectrum analyzer.

The DC to 3 Ghz spectrum is displayed on the PC screen seen in Figures 10, 11, and 12. The Digital Voltmeter (DVM) shown in Figures 10 and 11 is measuring the voltage drop across a 1 Ohm resistor on the test PCB, this giving an indication of the reduced dynamically induced, DC current flow with the CC_100 PO/SSC IC engaged (inserted) vs disengaged (extracted). In Figure 11, one sees an 8mA decrease in DC current flow and a broadband spectral reduction and modification in noise with the CC_100 engaged vs disengaged. Figures 11, 12, and 13 show this spectral reduction/modification, Figures 11 and 12 showing a close up of the spectral reduction with the CC_100 PO/SSC vs a standard MLCC 1 uF Electrolytic capacitor.

The 3 Ghz spectrum analyzer has the capability of outputting plot data into an excel spreadsheet and software has been developed that allow very detailed post analysis of multiple spectral inputs. An excerpt of this excel spreadsheet software is included in Figure 14. It has been shown that with the analysis software, that sensitivities as low as the delta in the dynamic activity of one CMOS inverter can be detected. Thus, subtle differences in the spectral behavior of the monolithic CC_100 PO/SSC design are detectable with this developed CC_100 PO/SSC IC test system.

If higher noise spectral bandwidths are required, a higher bandwidth Spectrum analyzer, such as the 6 Ghz Keysight N1996A-506 CSA, shown in Figure 15, can be rented and utilized.

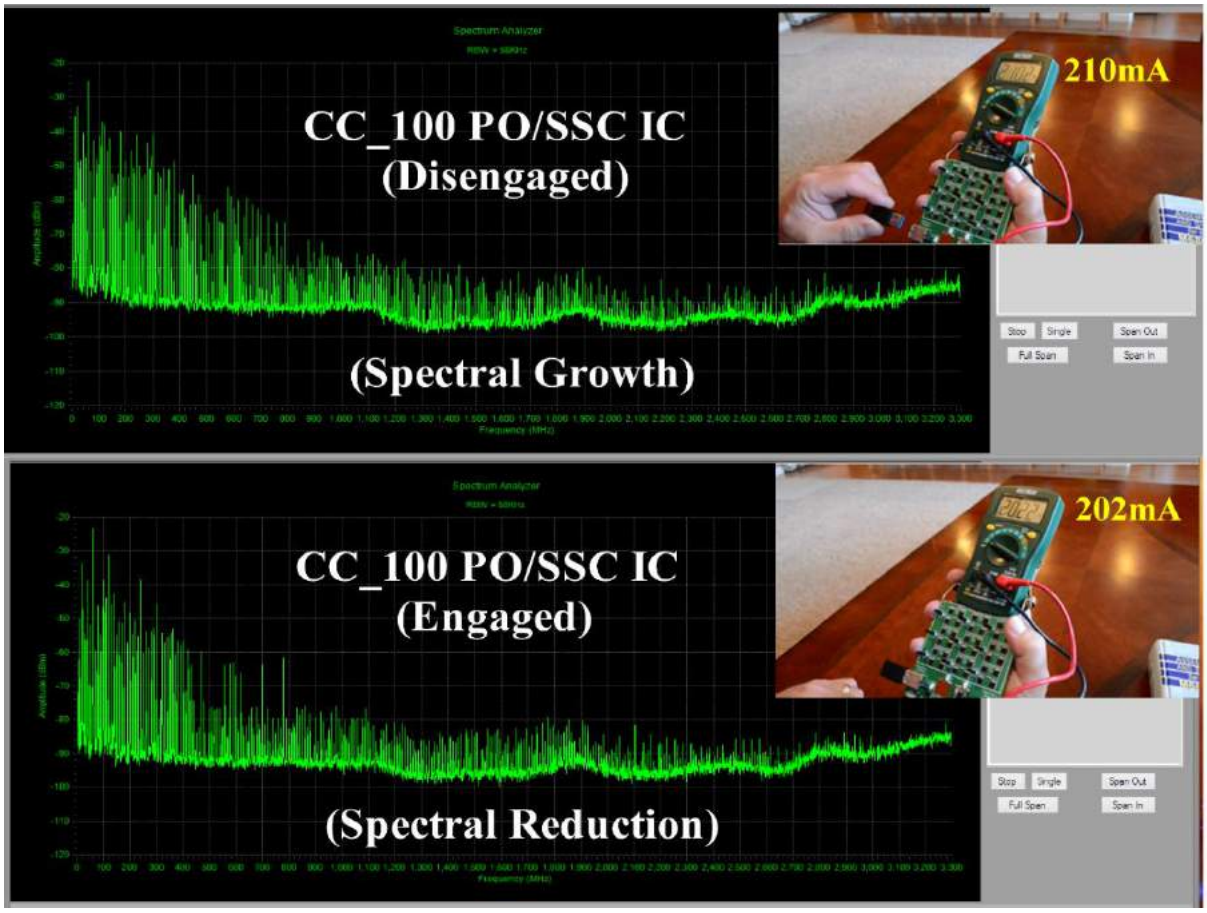


Figure 11: CC_100 PO/SSC IC/PowerStic/Exodus DC and Spectral Deltas

The plots shown in Figures 11, 12 and 13 show the dynamic power reduction produced by the monolithic CC_100 PO/SSC IC, utilizing the test system shown in Figure 10. Over 40 parts were tested from the prototype lot, with reference design and PowerStic/Exodus packaging, all measurement data showing a virtually identical pattern. Power Reduction DC measurements were shown to be identical, part to part, showing an 8mA delta, driven by the test system shown in Figures 10 and 11.

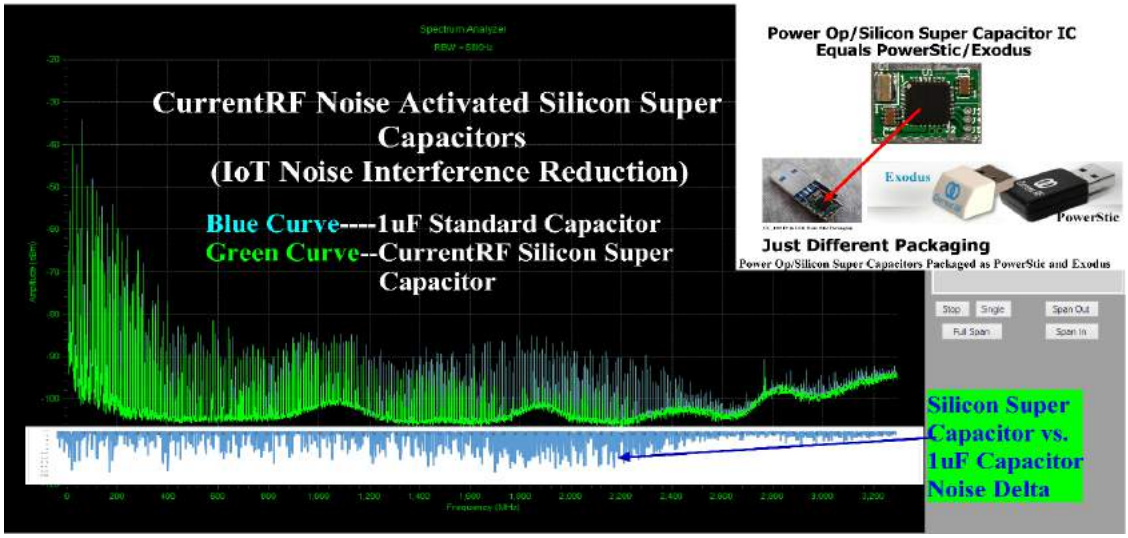


Figure 12: CC_100 PO/SSC IC/PowerStic/Exodus vs. 1uF Capacitor Spectral Power Deltas

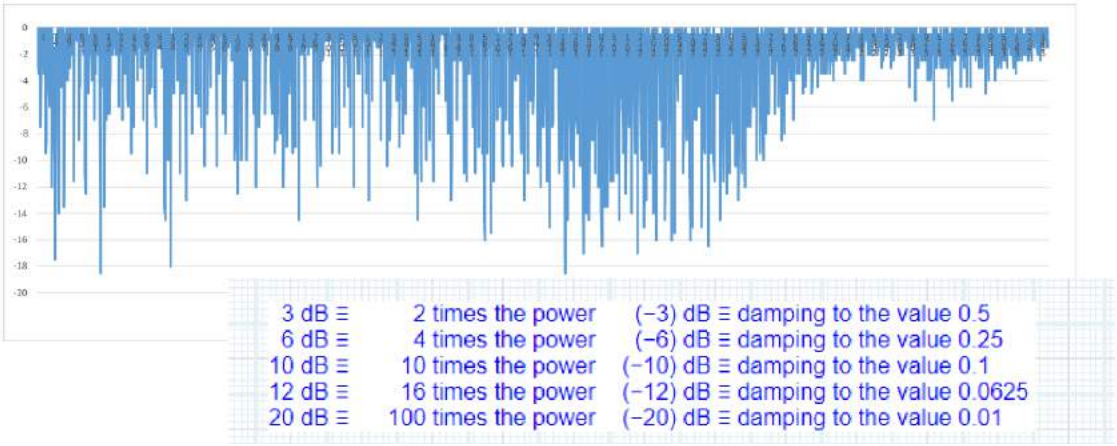


Figure 13: CC_100 PO/SSC IC/PowerStic/Exodus vs. 1uF Capacitor Spectral Power Reduction

Figures 12 and 13 show the supply noise spectral results of a standard 1uF electrolytic capacitor as compared to the noise spectrum that is the result of the monolithic CC_100 PO/SSC IC. The delta, shown in Figure 13, was generated by excel spreadsheet post processing of the 1uF Electrolytic capacitor spectral data and the monolithic CC_100 PO/SSC IC spectral data, an excerpt of this software shown in Figure 14.

3300.648	-95.391	-94.891	-0.5	2.89001E-13	3.24265E-13	-3.5264E-14	3.52635E-14	2.65569E-08	
3301.571	-95.402	-94.902	-0.5	2.8827E-13	3.23445E-13	-3.5174E-14	3.51743E-14	2.65233E-08	
3302.494	-95.413	-94.913	-0.5	2.87541E-13	3.22626E-13	-3.5085E-14	3.50853E-14	2.64897E-08	
3303.417	-95.925	-94.925	-1	2.55564E-13	3.21736E-13	-6.6172E-14	6.61721E-14	3.63791E-08	
3304.34	-94.936	-94.436	-0.5	3.20922E-13	3.60081E-13	-3.9158E-14	3.91585E-14	2.79852E-08	
3305.263	-94.948	-94.448	-0.5	3.20037E-13	3.59087E-13	-3.905E-14	3.90504E-14	2.79465E-08	
3306.186	-95.96	-94.96	-1	2.53513E-13	3.19154E-13	-6.5641E-14	6.56409E-14	3.62328E-08	
3307.109	-94.973	-94.473	-0.5	3.182E-13	3.57026E-13	-3.8826E-14	3.88263E-14	2.78662E-08	
3308.032	-95.485	-94.485	-1	2.82813E-13	3.56041E-13	-7.3228E-14	7.32276E-14	3.82695E-08	
						-4.5823E-08		0.002150034	approx. delta measurement of the dc meter (Idc)
Frequency (Mhz)	without dbm	with dbm	subtract dbm	without power (W)	with power (W)	summation subtract power (W)	absolute value	multiply by the approx input Z ratio spec an input to CC-100 input ratio of 10 to 1 (saved Current) I(rms)	

Figure 14: CC_100 PO/SSC IC/PowerStic/Exodus Statistical Analysis

1.5 CC_100 PO/SSC IC Small Signal Effective Capacitance Characterization

Monolithic CC_100 PO/SSC IC testing was not limited to Spectral Noise Plots and DC Power comparisons. CC_100 PO/SSC IC S11 Retrun Loss and reflection with respect to Power Integrity in system power grids are of interest. To this end, the CC_100 refernce board, shown in Figure 16, was modified and the Keysight N1996A-506 CSA shown in Figure 15, rented and procured, to do Return Loss and Spectrum testing.

Figure 15: Keysight N1996A-506 Spectrum/Network Analyzer

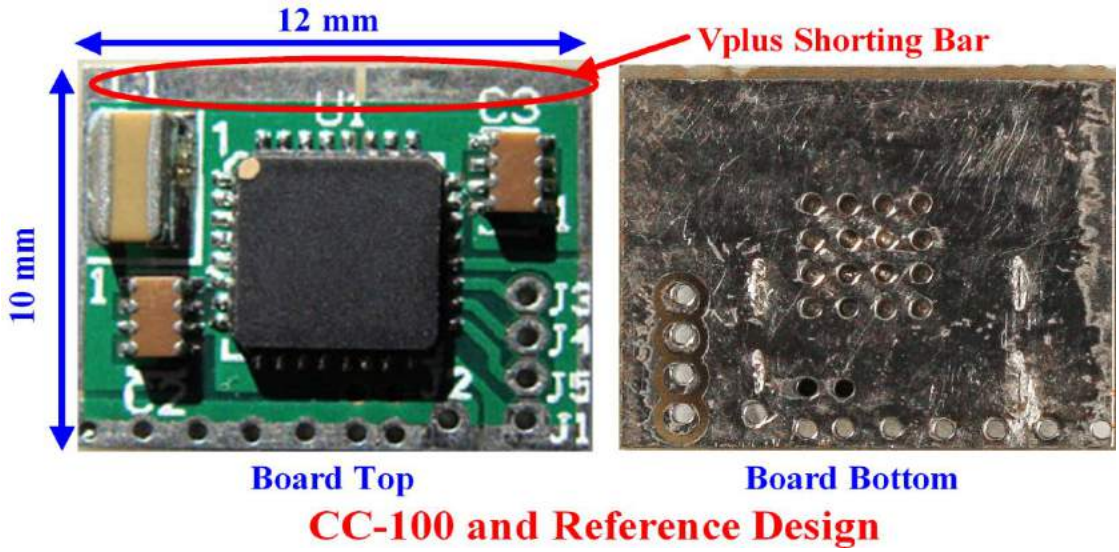


Figure 16: CC_100 PO/SSC IC Reference Design Utilized For Return Loss Testing

Figure 16 shows the CC_100 (U1), the C1 and C2 input capacitors (11uF total combined capacitance), and the C3 output capacitor (1 uF). With a nominal SPST switch, the Vplus shorting bar can be bridged and opened, creating the conditions for the plots generated with the Keysight N1996A Network/Spectrum Analyzer shown Figure 15, the plots shown in Figures 17 through 20.
Observing the Figure 17 through 20 S11 plots, one can see the 2X effective small signal capacitance increase due to CC_100 PO/SSC dynamic action. This 2X small signal effective capacitance increase is explained below.

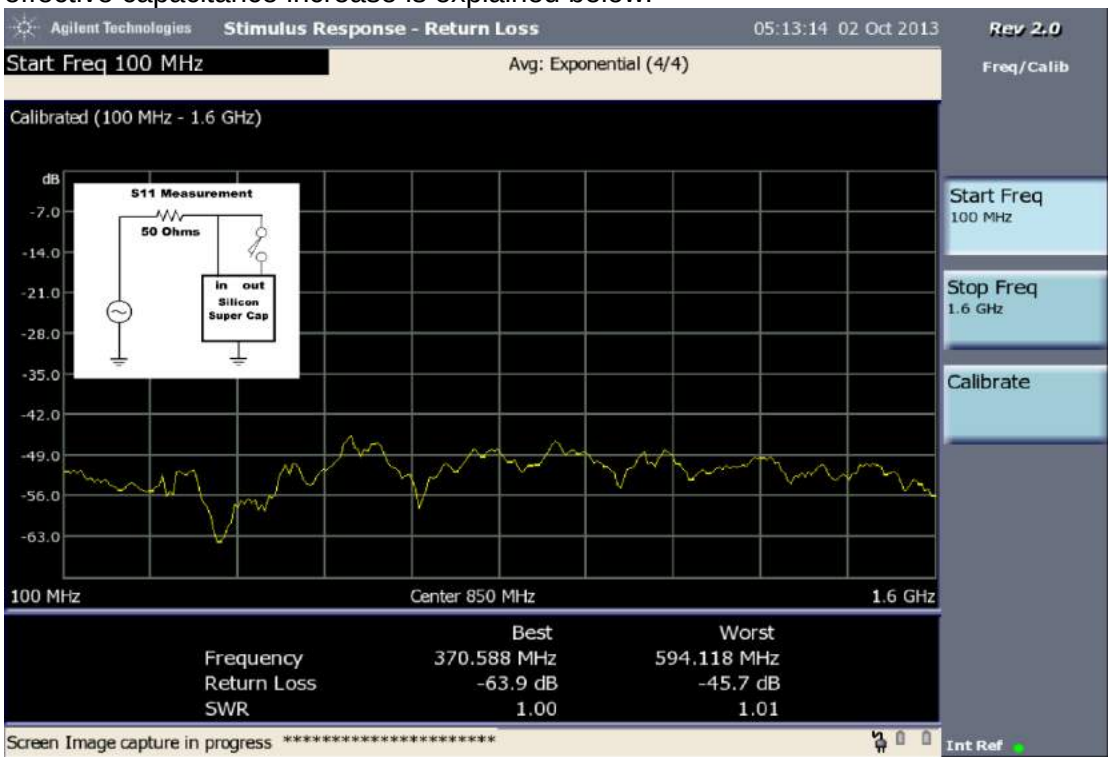


Figure 17: CC_100 PO/SSC Small Signal S11 Disengaged Input Return Loss- Lowest Impedance Point- 370Mhz

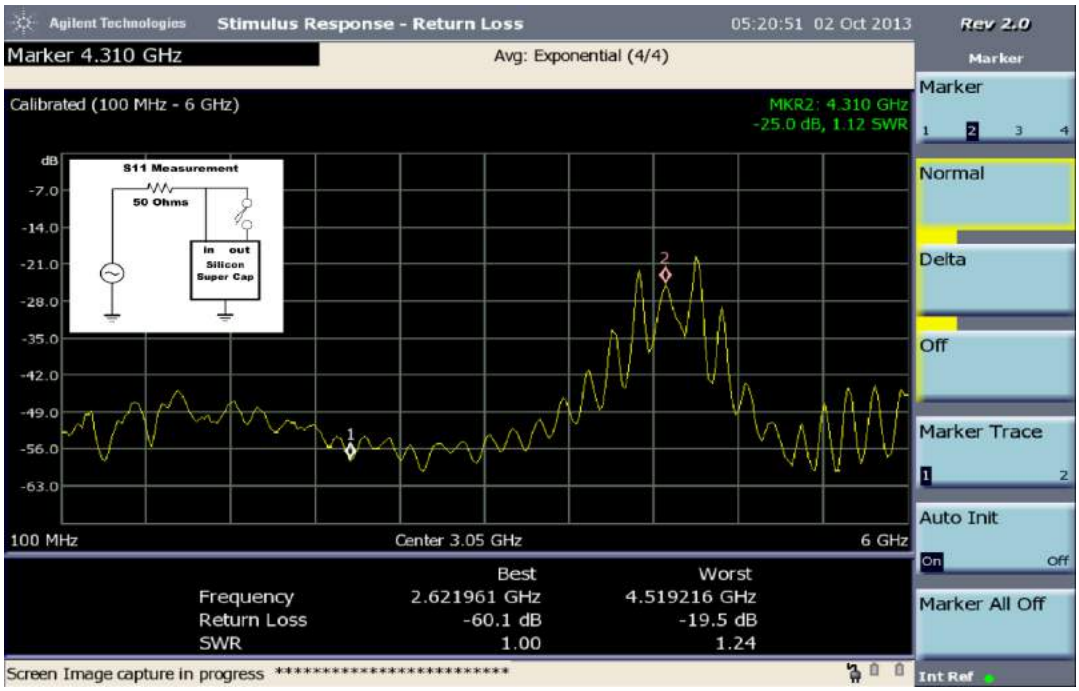


Figure 18: CC_100 PO/SSC Small Signal S11 Disengaged Wideband Input Return Loss

In Figure 17, the return loss/SWR and the lowest impedance point occurs at 370Mhz (-64dB) and corresponds to a capacitive low impedance magnitude of 39 Micro Ohms. A short math proof is as follows.

Equation 1:

$$50 * invlog\left(-\frac{dB}{10}\right) \cong 1/(2 * \pi * f * C)$$

Using the Silicon Super Cap IP data, the lowest impedance point frequency in the Figure 17 plot, as well as the “Best” return loss and SWR numbers from the Network Analyzer, gives:

$$50 * invlog(-\frac{63.9dB}{10}) \cong 1/(2 * \pi * 370Mhz * 11uF)$$

Solving yields:

$$20\mu\Omega \cong 39\mu\Omega$$

Which, within measurement and error tolerances, the results are essentially equal. Figure 18 shows a wideband version of the Figure 17 return loss plot. In the Figure 18 plot, one sees a resonant rise in reflection, thus impedance, at 4.3 Ghz.

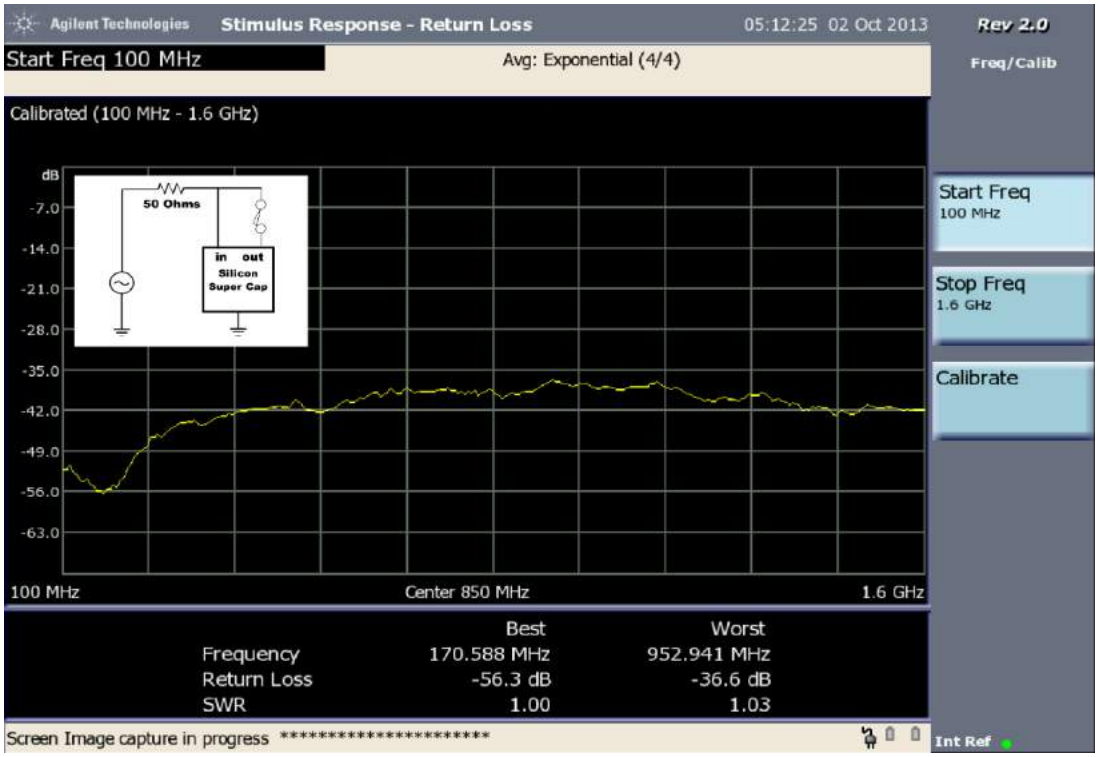


Figure 19: CC_100 PO/SSC Small Signal S11 Engaged Return Loss- Lowest Impedance Point- 170Mhz

Referencing Figure 19, using the same base input capacitance, 11uF, shown in Figure 3, and engaging the CC_100 PO/SSC chip, the best return loss/SWR the transfer function lowest impedance point is translated down to 170Mhz(-56.3dB). Accounting for a +7 dBm scaling with respect to the Figure 17 and 19 plots, this due to return currents flowing from the Silicon Super Capacitor IP output into the Network Analyzer detectors, the low impedance point corresponds to a capacitive low impedance of 42 Micro Ohms. This low impedance dip in Figures 19 and 20 fits the impedance and frequency characteristic that would be seen utilizing a standard 22uF capacitance (2X the static input capacitance). This measurement confirms the effective capacitance increase generated by the action of the Silicon Super Capacitance Chip. The math for this condition as follows.

Equation 2:

$$50 * invlog((-dB - 7dB)/10) \cong 1/(2 * \pi * f * C)$$

Using the Silicon Super Cap Chip data, the lowest impedance point frequency in the Figure 19 and 20 plots, as well as the “Best” return loss and SWR numbers from the Network Analyzer gives:

$$\left(50 * invlog\left(\frac{(-56.3dB - 7dB)}{10}\right)\right) \cong 1/(2 * \pi * 170Mhz * 22uF)$$

Solving yields:

$$23.4\mu\Omega \cong 42\mu\Omega$$

Which, within measurement and error tolerances, the results are essentially equal.

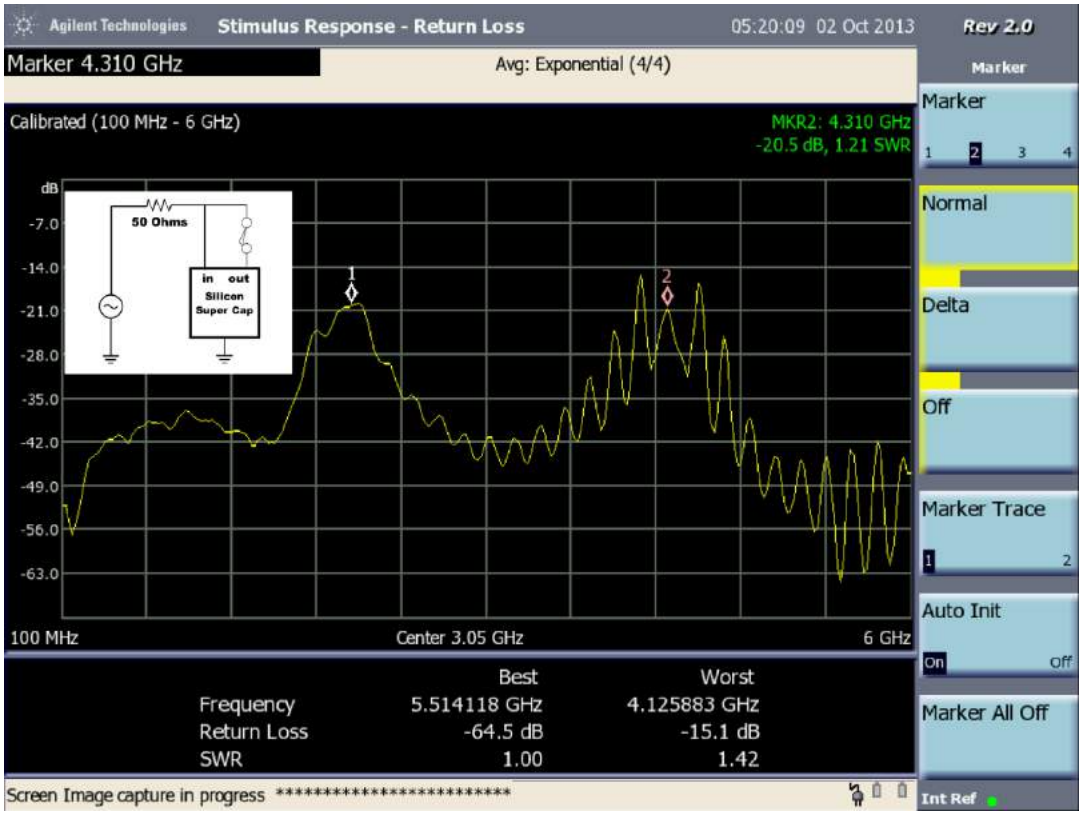


Figure 20: CC_100 PO/SSC Small Signal S11 Engaged Wideband Input Return Loss

Figure 20 shows a wideband version of the Figure 19 return loss plot. In the Figure 20 plot, one sees the resonant rise in reflection, thus impedance, at 4.3 Ghz.

1.6 CC_100 PO/SSC IC Large Signal Reservoir Capacitance Characterization

Figure 21: CC_100 PO/SSC IC/PowerStic/Exodus Portable Test System

Large signal dynamics measurement generally requires a test system that can expose a device under test (DUT) to large signal stimulus (greater that 25mV pp). The test system shown in Figure 21 has this large signal stimulus capability, and can be adjusted in discrete magnitude levels of stimulus noise. This being the case, the Figure 21 test system can be utilized for large signal reservoir capacitance testing for the CC_100 PO/SSC IC.

CC_100 PO/SSC IC large signal, reservoir capacitance increases by at least 2X with applied noise and tracks input noise magnitude, when the PowerOp/SSC Chip is stimulated with increasing levels of dynamic current. The reservoir capacitance increases as the dynamic current applied increases. With no dynamic current applied, the reservoir capacitance is 1uF, what one would get with Standard MLCCs. When dynamically activated, the large signal, reservoir capacitance will increase as the input noise increases, as in the Figure 22 through 25 data examples. With moderate increases in noise levels above small signal (25mVpp), the on chip reservoir capacitance increases at least 2X over the static value, or an increase to 2uF as the result of CC_100 PO/SSC action seen in Figures 17 and 19 above.

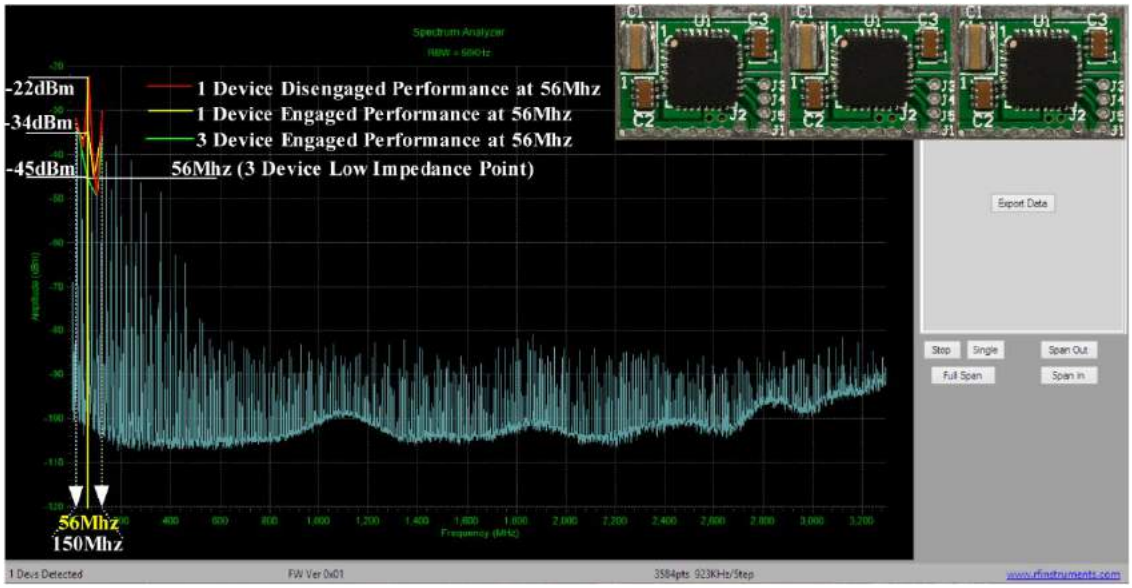
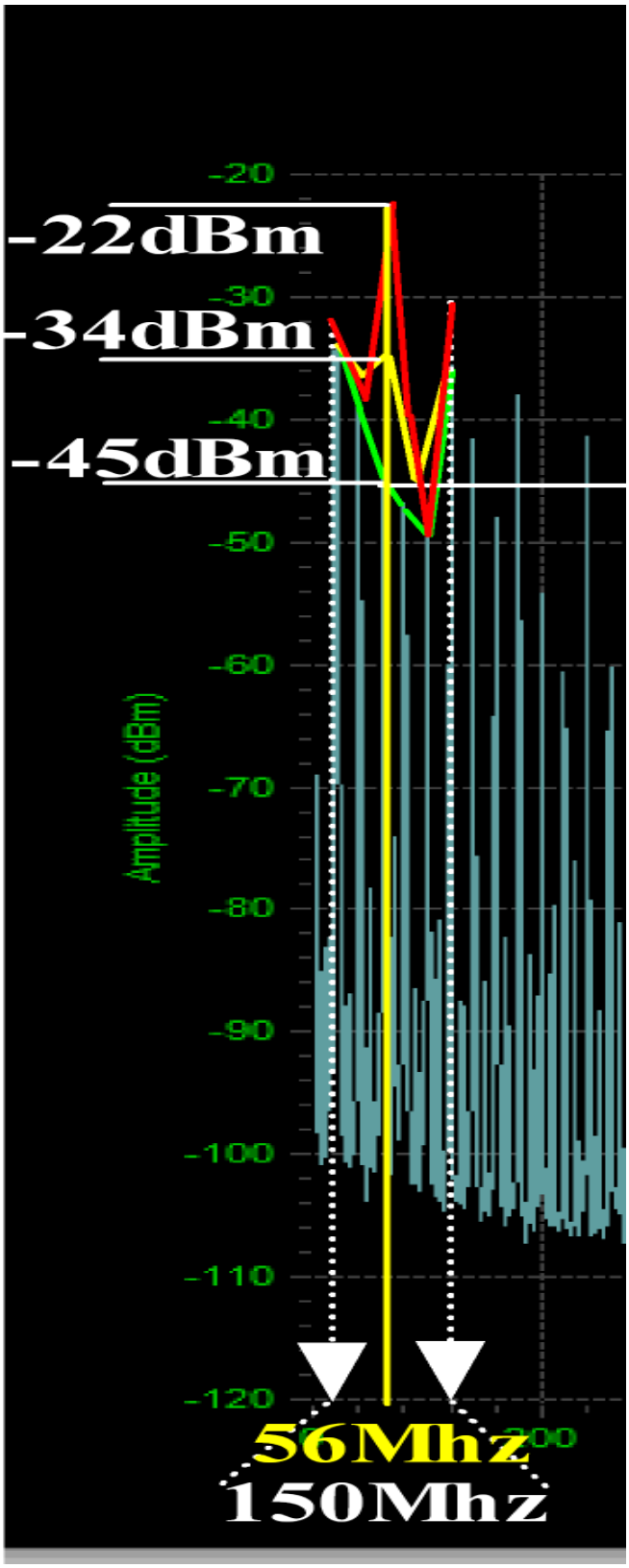


Figure 22: CC_100 OP/SSC Large Signal Reservoir Capacitance Dynamics

Figures 22 and 23 show the large signal behavior described above. Using the low impedance point shown for single, engaged PowerOp/SSC Chip, shown in Figures 17 and 19, as a baseline measurement, the lowest impedance point for 3 parallel connected CC_100 PO/SSC Chips, moves from 170Mhz to 56Mhz(a factor of 3 reduction in frequency) and a ~ 6 to 7 dB magnitude reduction is realized.

Figures 22 and 23 show a supply noise spectrum generated by the Pseudo Random Test system and CC_100 PO/SSC IC shown in Figure 21 with 3 parallel connected CC_100 PO/SSC Chips. Figure 23 shows a close up of the lowest impedance point (56Mhz), the green curve superimposed on the spectral noise plot showing the effect of the 56Mhz low impedance point on the overall noise spectrum generated with the 3 engaged parallel CC_100 PO/SSC Chip instances. As Figures 22 and 23 show, the magnitude of the frequency content at 56Mhz for the 3 parallel CC_100 instances is -45dBm.

The yellow, 56Mhz superimposed curve in Figures 22 and 23 shows the magnitude of the frequency content centered at 56Mhz for one engaged PowerOp/SSC Chip. As shown in Figures 17 and 19, the single chip lowest impedance point moves to 170Mhz, thus the magnitude of the spectrum centered at 56Mhz moves up ~12 dB to -34dBm.



The red, 56Mhz superimposed curve in Figures 22 and 23 shows the magnitude of the frequency content centered at 56Mhz for one disengaged PowerOp/SSC Chip. Referring back to Figures 17 and 18, the disengaged, single chip lowest impedance point moves to 370Mhz, thus the magnitude of the spectrum centered at 56Mhz moves up another ~12 dB to -22dBm.

Thus, the spectrum data shown in Figures 22 and 23 yield an additional 6dB drop on top of the nominal small signal 6db magnitude reduction shown with the small signal network analysis shown in Figures 17 and 18. This additional 6 dB spectral magnitude reduction is the result of supply line noise magnitudes greater than small signal (noise magnitude 50 mVpp in this case), and is caused by the inherent energy harvesting occurring within the CC_100 PO/SSC device. This behavior is reflective of a reservoir capacitance increase that is resultant of higher than small signal noise magnitudes (25mVpp) being input to the device from the supply line. Since dynamic reservoir capacitance does not behave in the same manner as nominal capacitance (generally, the larger the nominal capacitance, the lower in frequency the capacitive response becomes), greater capacitive cancellation and reservoir effects are seen to increase as supply line noise signal increases.

The rms delta in current shown in the Figures 22 and 23 plots is 3.45mA, that ranging from the disengaged red curve to the 3 parallel engaged devices (the green curve). Thus, the larger the noise input magnitude with the CC_100 PowerOP/Silicon Super Capacitor, the greater the reservoir effects become.

Figure 23: Large Signal Dynamics

Figures 24 and 25 show CC_100 response to a high power impulse and the resulting increased reservoir capacitance effect (Figure 24) as supply line noise increases. As the Figure 24 and 25 plots show, a 142mA delta exists (a 36% dynamic current reduction with respect to the CC_100 PO/SSC IC disengaged condition) between the disengaged and engaged impulse response plots, Figure 26 showing the scaling that exists between the device input current and reservoir capacitance the IP generates. Thus, with greater noise magnitudes on system supply lines, the CC_100 PO/SSC Chip outputs greater reservoir currents to cancel the noise impulses that are input to the IP.

The mathematics for this reservoir effect are simple:

Equation 3:

$$Ic = C(\frac{dv}{dt})$$

Rearranging:

$$\frac{Ic}{\frac{dv}{dt}} = Creservoir$$

For the PowerOp/SSC Chip case:

$$\frac{Ic}{15625000} = Creservoir$$

The dv/dt substitutions above are generated from confidential CC_100 PO/SSC device parameters

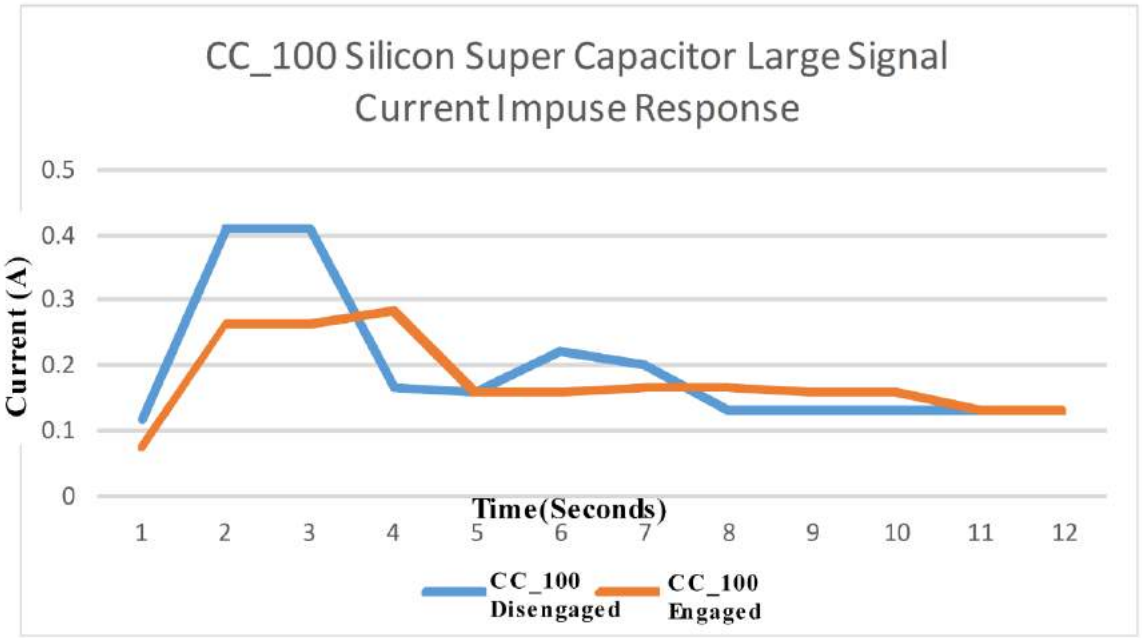


Figure 24: CC_100 PO/SSC Chip Disengaged/Engaged High Current Impulse Response

Figure 24 shows the CC_100 PO/SSC Chip response to high current impulses. The **blue** plot in Figure 23 shows a typical system response to an increased load current demand from system regulators. Not only is the CC_100 PO/SSC IC disengaged impulse magnitude higher than the brown engaged plot in Figure 23, the plot demonstrating a current reduction of 36%, the disengaged plot shows a higher degree of ringing, moving toward an underdamped system response, with respect to the engaged plot. The Figure 24 plot also shows the effect of the negative feedback of the energy harvesting embedded in the CC_100 PO/SSC and it's effect on system stability. The PO/SSC IC injects recharging current in response to the supply line voltage perturbation that is the result of system load current increases, effectively canceling a portion of the initial induced supply line voltage disturbance. One could also say that the increased reservoir capacitance from the IP does a better job of filtering the result of instantaneous load current increases.

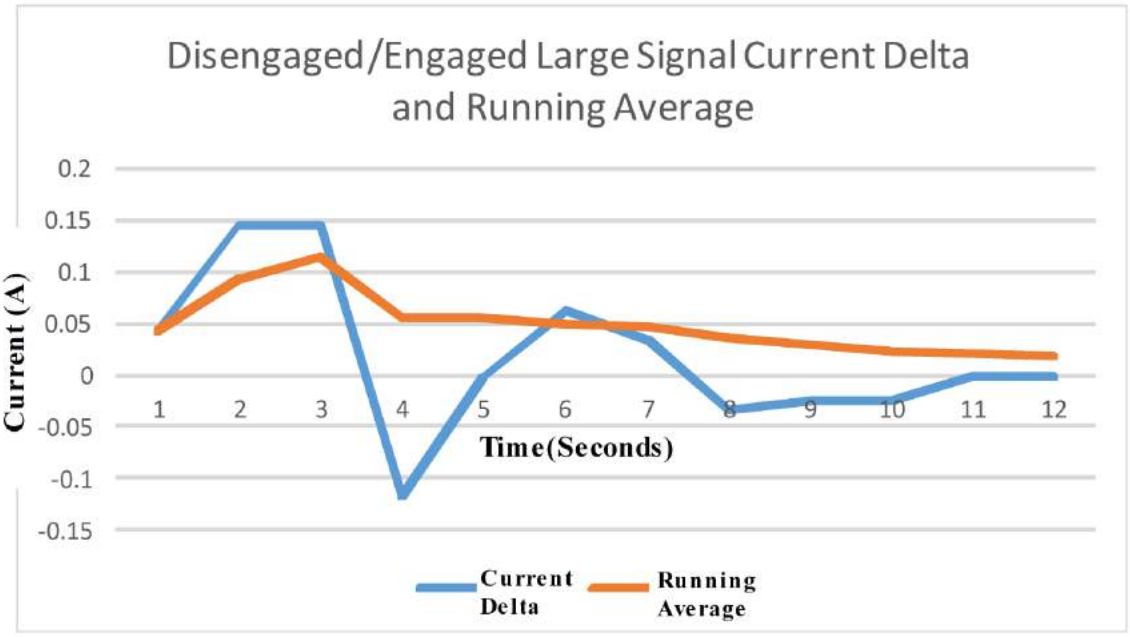


Figure 25: CC_100 PO/SSC Chip Current Delta with Running Average

Figure 25 shows the current disengaged/engaged delta and running current delta average for the Figure 24 plot. The positive excursions above zero current in Figure 25 is the result of current injected from the PowerOp/SSC Chip to cancel the induced voltage perturbation and supply the current created by the load current impulse demanded by the circuit load, the negative excursions below zero current in the plot, the result of supply line ringing in response to the initial current impulse from the circuit load. One will notice that the current delta finally settles to zero current after 11 seconds, showing that the CC_100 PO/SSC Chip responds only to dynamic current perturbations, and the running average showing an overall positive current and power savings.

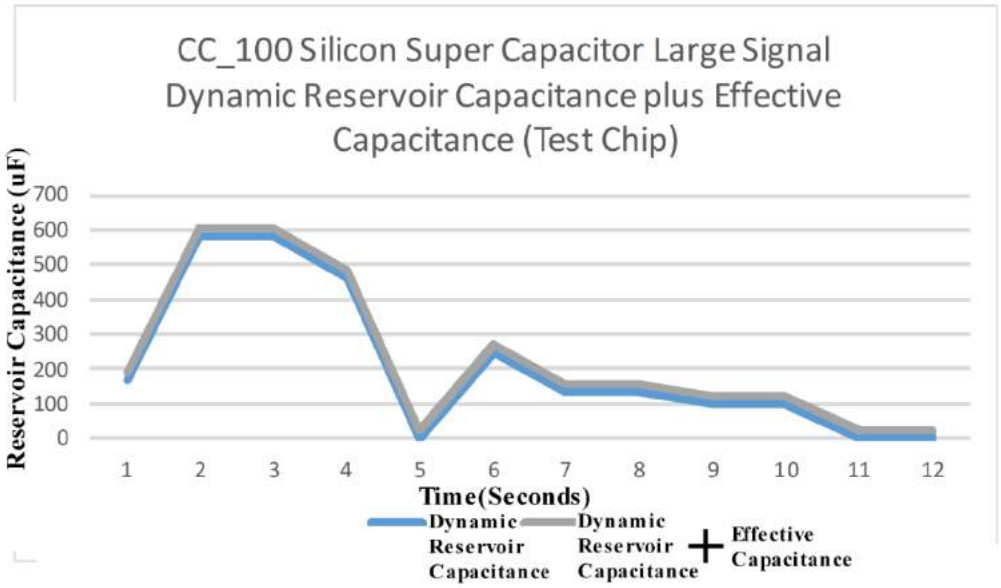


Figure 26: CC_100 PO/SSC Chip Dynamic Reservoir plus Effective Capacitance Test Chip Performance (1uf Static Output Capacitance)

Figure 26 shows the total CC_100 PO/SSC Chip dynamic reservoir and effective capacitance increases that are the result of the load current impulses imposed on the system supply grid and the PO/SSC Chip. The **grey** curve is the combination of the dynamic reservoir and effective capacitance, or total capacitance that the design generates in response to high current impulses, the **blue** curve is the dynamic reservoir capacitance alone. As one can see, the dynamic reservoir capacitance magnitude far outweighs the effective capacitance, and the dynamic reservoir capacitance driven by the magnitude of input dynamic current and supply voltage perturbations.

With a 1uF static output or return capacitance used on the CC_100 PO/SSC Chip and reference design, the magnitudes of the reservoir capacitance approach 1mF. This is an order of magnitude increase with respect to the capacitance provided by standard MLCCs. This is a good example of how the CC_100 PO/SSC Chip can dynamically enhance supply bypassing at the PCB level of integration.

So**,** the 2X increase in effective capacitance, the dynamically controlled increases in large signal, reservoir capacitance, the 25% reduction in ESL, and the resulting 36% drop in overall dynamic current and power draw, leads to better high frequency (lower ESL) and low frequency (higher Effective and Reservoir Capacitance-- leading to better filtering capability) filtering (broader dynamic range), and an up to 36% reduction in dynamic power draw. These characteristics lead to lower RF emissions from power grids, cleaner internal chip supplies, smaller DCAP footprints(if filtering area is a concern) lower chip dynamic power dissipation(lower thermal footprint), and greater circuit capacity.

2.0 CC_100 PO/SSC IC BIST Dynamic Noise Generation Testing

Figure 27 below shows the schematic details of the CC_100 PO/SSC IC Demonstration Platform. The Platform is constructed in such a manner that one only needs the materials outside of the **blue** polygon in Figure 27. An adjustable 1.65V to 1.9V power supply, and a DVM capable of DC micro-volt resolution is all that is needed to evaluate the CC_100 PO/SSC IC on this platform. The actual lab test setup is shown in Figure 28.

The Demonstration Platform utilizes ten, .18um, 1.8V logic gates, configured as a thermometer decoder embedded in the CC_100 PO/SSC IC, as circuitry utilized as a BIST Noise Test generator (see Figure 28). There are no 1.8V supply DCAPs inside the CC_100 PO/SSC IC, thus high frequency noise energy is output to the C1, C2, and C3 caps on the CC_100 PO/SSC IC reference design(see Figure 3), enabling CC_100 PO/SSC IC current and power reduction operation.
Typical CC_100 PO/SSC IC performance metrics are summarized in Figure 27 and shown in Table 4, showing that the performance of the CC_100 PO/SSC IC will change with supply variation (the output slew rate of the CC_100 PO/SSC IC internal logic varies with supply voltage) and with the slew rate and duty cycle characteristics of the onboard clock generator.
The CC_100 PO/SSC IC power reduction performance is seen to vary from around 5% supply current reduction to over 24% with proper lab setup.

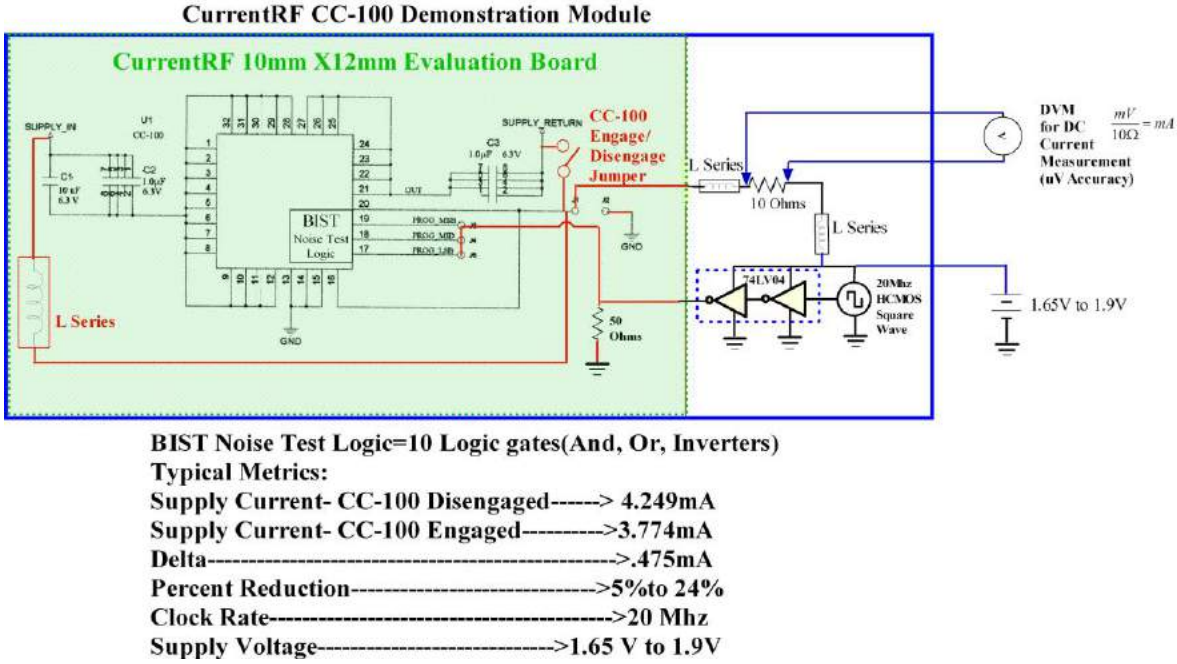


Figure 27: CC_100 PO/SSC IC Demonstration Module and Typical Metrics

Supply Voltage (V)	CC-100 PO/SSC IC Engaged (mA)	CC-100 PO/SSC IC Disengaged (mA)	delta (mA)	Percentage Reduction
1.9	5.392	5.88	0.488	8.3
1.85	4.932	5.233	0.301	5.7
1.8	3.774	4.249	0.475	11.17
1.75	2.717	2,858	0.141	5
1.7	1.997	2.113	0.116	5.5
1.65	1.106	1.464	0.358	24.4
				(Average)
				9.8

Table 4: CC-100 PO/SSC IC Demonstration Module

Performance Variance with Supply Voltage (aka Slew Rate)

Table 4 above shows CC_100 PO/SSC IC performance over varying supply voltages (1.9V to 1.65V) with the CC-100 PO/SSC IC engaged(the black jumper installed in Figure 28) and disengaged(the black jumper in Figure 28 de-inserted(not shown)). With the gathered raw data, the engaged/disengaged current delta and percentage current reduction with the engaged CC_100 PO/SSC IC is computed and inserted into Table 4. The Table 4 data was gathered with a Fluke 289 True RMS Multi-meter which possesses a micro-volt precision DC DVM. A micro-volt precision DC DVM is necessary for accurate CC_100 PO/SSC IC BIST testing.

Table 4 shows somewhat high variability in the current saved by the CC_100 PO/SSC IC(5% to 24%). This is not a variation in CC_100 PO/SSC IC performance, but is the result of slew rate variation in the onboard BIST generator and external clock generation circuits.

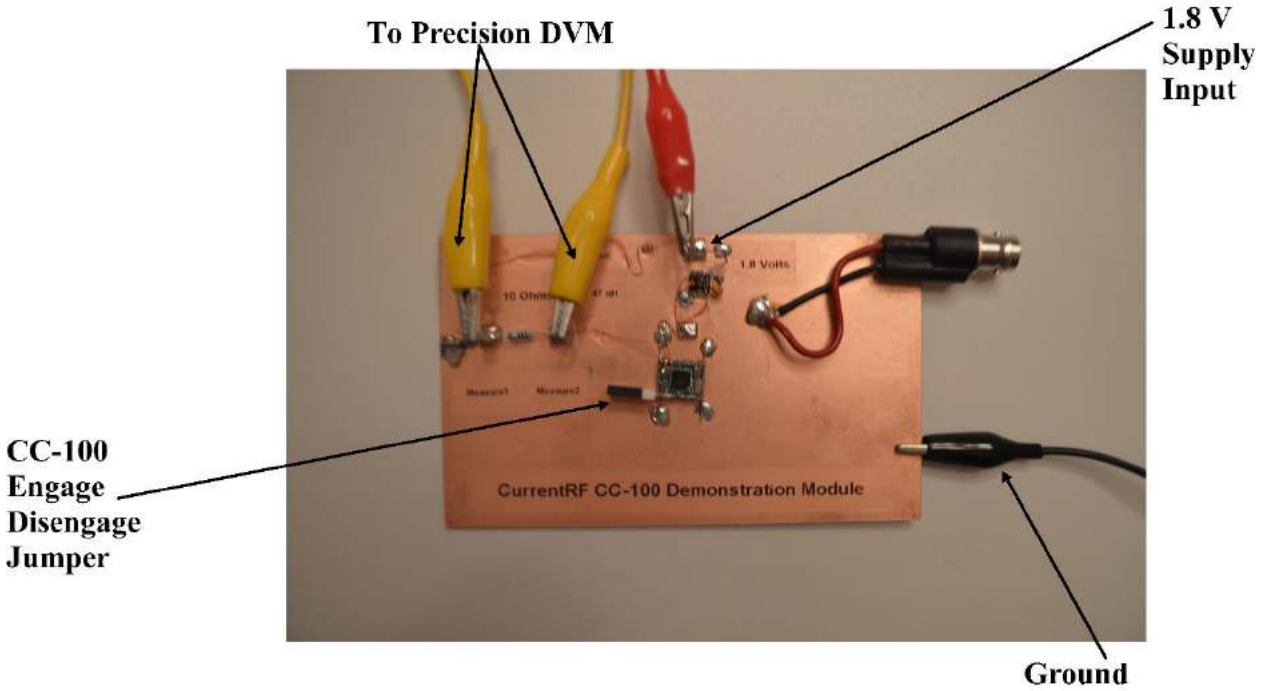


Figure 28: CC_100 PO/SSC IC Demonstration Module Set-Up

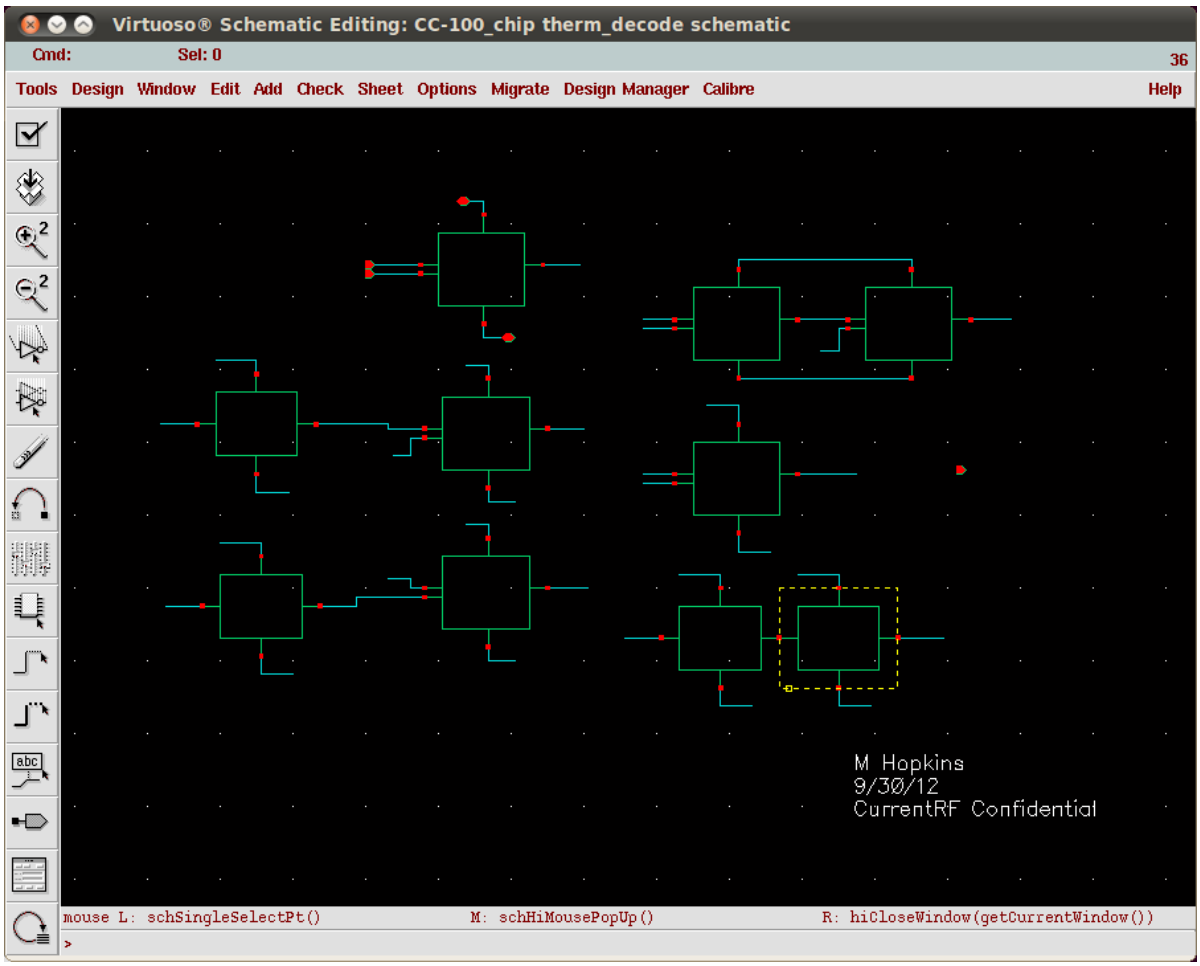


Figure 29: CC_100 PO/SSC IC Demonstration Module BIST Decoder Logic

Figure 29 above shows the CC_100 PO/SSC IC Thermometer Decoder used as a BIST Noise Engine for the CC_100 PO/SSC IC tests. Not shown are ESD cells with 250 Ohm resistor in series with the logic gate inputs and the pF range capacitances associated with the decoder inputs.

3.0 Paypal PowerStic-CC_100 PO/SSC IC Testing

Methodologies and techniques described below were utilized to monitor and measure three HP Proliant DL560 Gen 8 Paypal data servers with and without the PowerStic-CC_100 PO/SSC ICs inserted into server USB ports. All power reduction data is due to the insertion of the PowerStic-CC_100 PO/SSC IC into empty USB server ports. More power could be saved if the CC_100 PO/SSC IC were inserted into the main mother boards of the tested HP Proliant DL560 Gen 8 Paypal data servers.

3.1 USB Port Spectrum Tests

The first test was a USB spectrum test, used to determine the amount of circuit noise present on the port, the setup shown in Figure 30. Since USB Ports are power and ground parallel connected, inserting and extracting the PowerStic-CC_100 PO/SSC IC

was a quick check of the amount of power present on the port and how much power the PowerStic-CC_100 PO/SSC IC saves in systems.

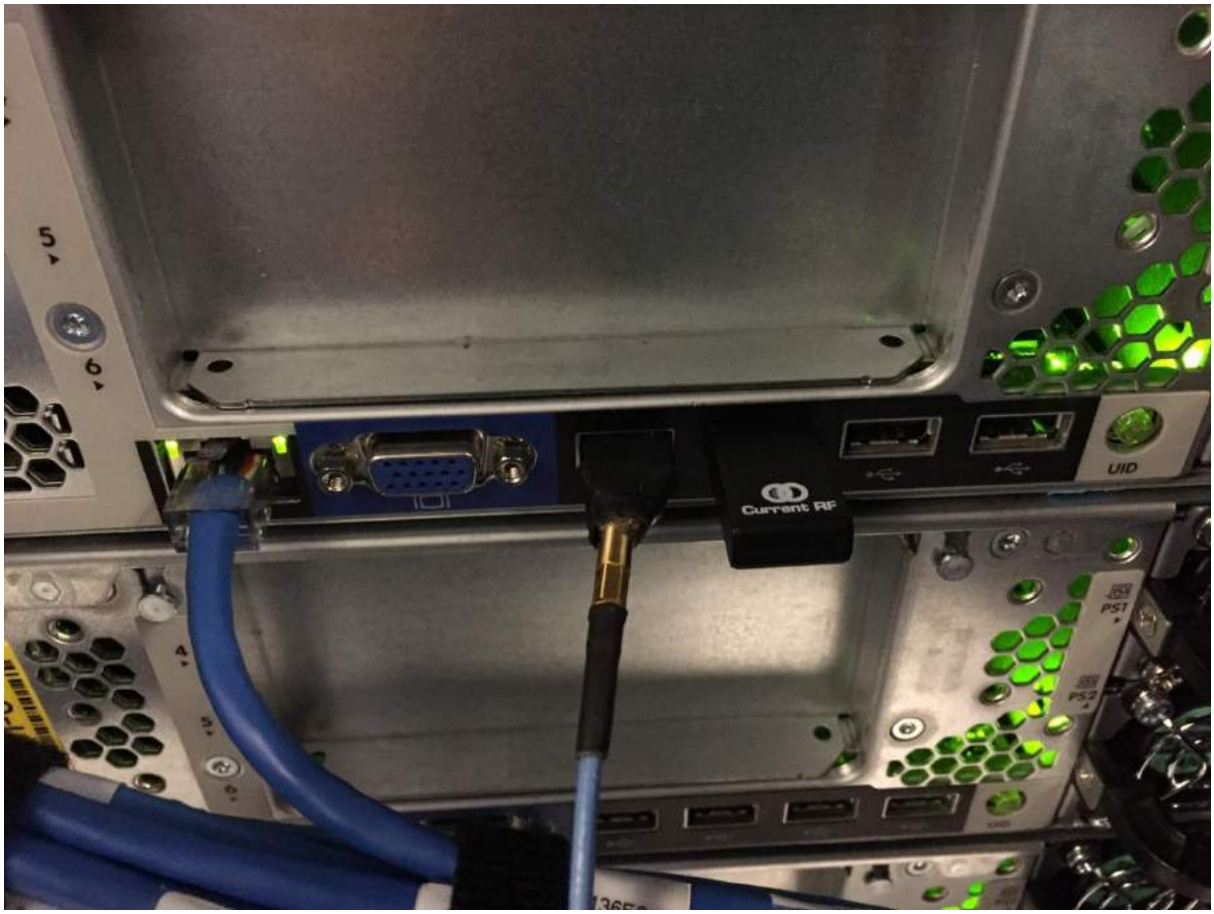


Figure 30: USB Spectrum Measurement Setup

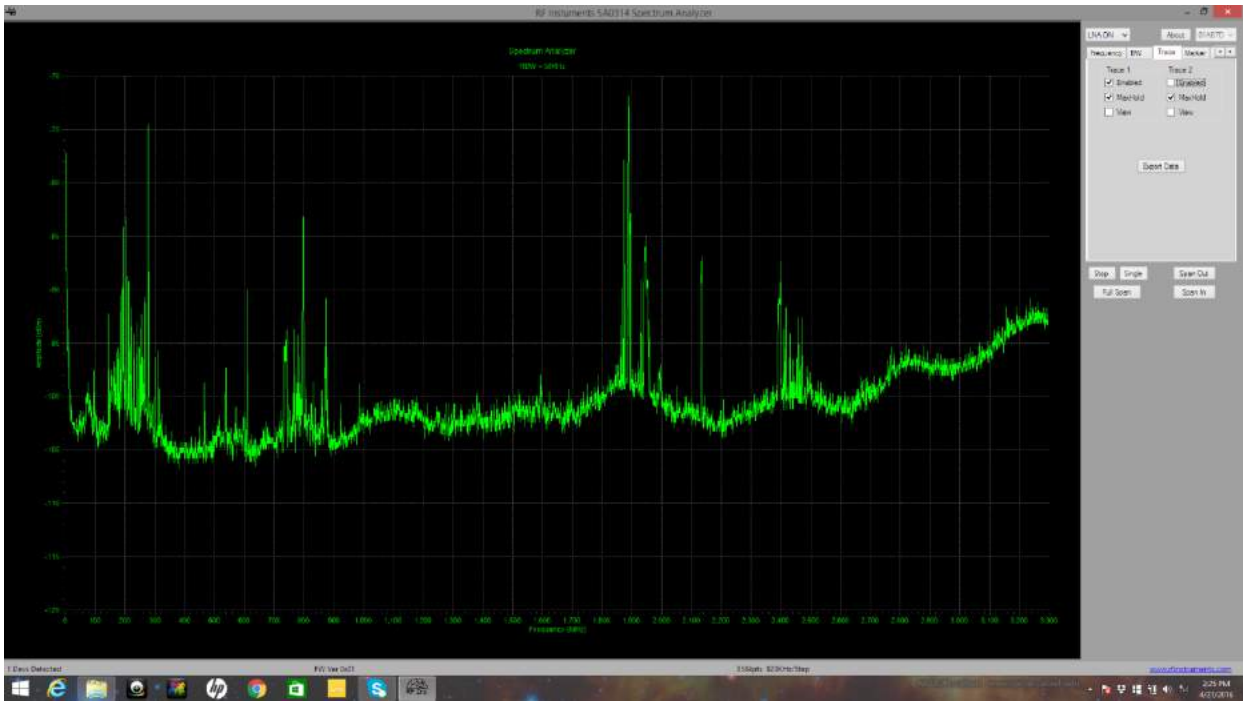


Figure 31: USB Spectrum Measurement-PowerStic-CC_100 PO/SSC IC Extracted

The spectral plot in Figure 31 shows the energy coupled to the USB port from inside the HP Proliant DL560 Gen 8 Paypal data server. The Figure 32 plot shows the energy reduction and resulting power savings when the PowerStic-CC_100 PO/SSC IC device is inserted into the USB port as shown in Figure 30. The delta shown in the Figure 32 plot in relation the power displayed in the Figure 31 plot shows the potential savings when the PowerStic-CC_100 PO/SSC IC is inserted into a server USB port.

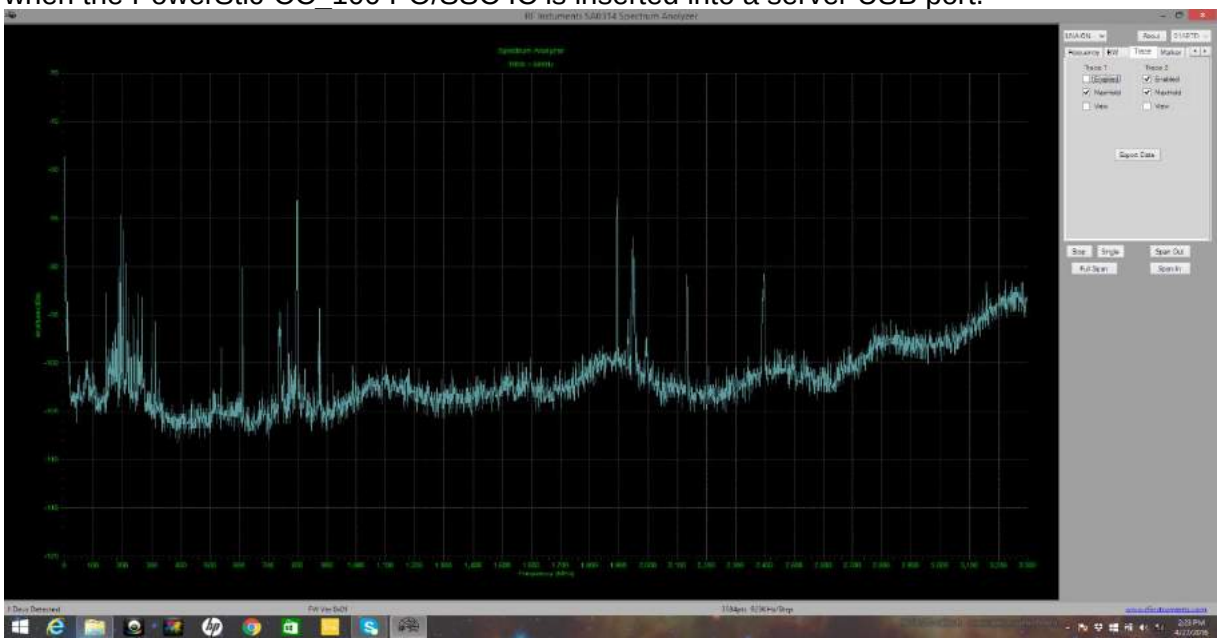


Figure 32: USB Spectrum Measurement-PowerStic-CC_100 PO/SSC IC Inserted

3.2 Wall Plugged PowerStic-CC_100 PO/SSC IC Tests

Figure 33: 24 Hour Example PowerStic-CC_100 PO/SSC IC Extracted Plot

Based on the spectral results shown in Figure 32, the decision was made to do further long term testing on three HP Proliant DL560 Gen 8 Paypal data servers(servers 016, 019, 020 data shown in Figures 33 to 38 below). It was decided to do a 24hr test in a temperature controlled server facility, without the PowerStic-CC_100 PO/SSC IC inserted as a server baseline measure, using Paypal's resident power measurement equipment, then repeat the test the following 24hr day under temperature controlled conditions, with the PowerStic inserted into the server USB port. This 24hr off/24hr on routine was repeated 5 times, results plotted and recorded each day and representative sample plots shown in Figures 33 and 34 below.

Figures 33 and 34 show example 24 hour plots of the power drawn by server 016 without and with the PowerStic inserted, respectively. Data is taken in 15 minute intervals during the 24 hour recording period for each plot. Scanning over the Figure 33 and 34 plots, one can see fewer peaks in the extracted plot in Figure 32 than is seen in the Figure 33 Inserted plot. This is not due to PowerStic-CC_100 PO/SSC IC performance, but is the nature of the data processing and OS variation in and on the server on given recording days.
The sampled and computed average of each plot is the important parameter here. When sampled and computed, the average power for the Figure 33 PowerStic-CC_100 PO/SSC IC extracted plot is 292 Watts (2nd extracted row entry in Table 2). The computed average power for the Figure 34 PowerStic-CC_100 PO/SSC IC inserted plot is 270 Watts(2nd inserted row entry in Table 2), showing average difference of 22 Watts

between the 2 recording days and conditions. Thus, given long term power recording runs, the peak to peak variations of the data processing and OS drop out, revealing the true performance of the PowerStic-CC_100 PO/SSC IC device in server systems.

Figure 34: 24 Hour Example PowerStic-CC_100 PO/SSC IC Inserted Plot

3.3 Statistical Data Analysis

Figure 35 shows a 4 day sampled composite Histogram of the Paypal 016, 019, and 020 data servers with and without the PowerStic-CC_100 PO/SSC IC inserted in each machine. The blue data (PowerStic-CC_100 PO/SSC IC Inserted) and power average shows substantially lower power than the PowerStic-CC_100 PO/SSC IC Extracted data (brown). The data shows an approximate normal distribution, with the standard deviations being 13 to 17 watts with the PowerStic-CC_100 PO/SSC IC Inserted average being 276 Watts per hour per server, and the PowerStic-CC_100 PO/SSC IC Extracted average being 286 Watts per hour per server, a difference of 10 Watts per hour per server, or 3.5% in Paypal systems.

Multiplying this 10 watt PowerStic-CC_100 PO.SSC IC created difference by 24 hrs per day and then by 30 days in a month, one arrives at 7.2 Kilowatts saved per month per server.

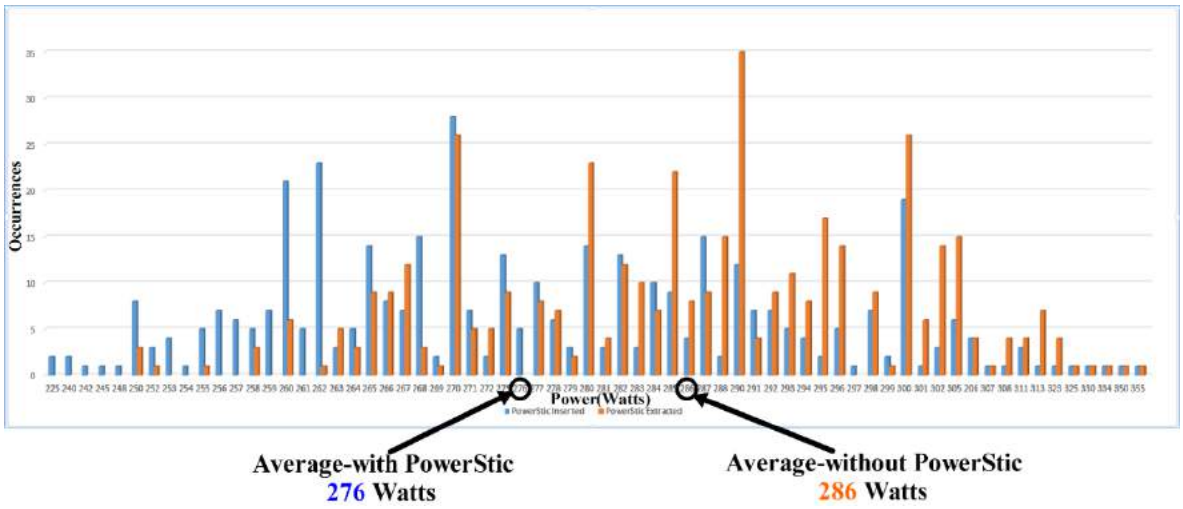


Figure 35: Three HP Server Savings Composite Histogram Average Savings-10 Watts/Server/Hour

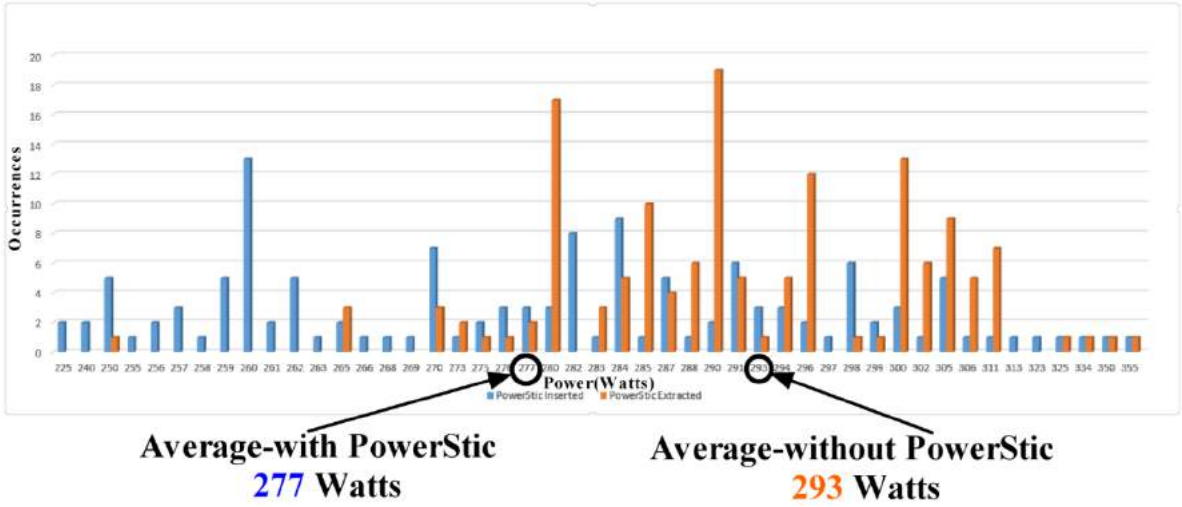


Figure 36: Server 016 Savings Composite Histogram 16 Watts/Server/Hour

Figure 36 shows a 4 day sampled composite Histogram of server 016 with and without the PowerStic-CC_100 PO/SSC IC inserted in the 016 machine. The blue data (PowerStic-CC_100 PO/SSC IC Inserted) and power average shows substantially lower power than the PowerStic-CC_100 PO/SSC IC Extracted data (brown). The data shows an approximate normal distribution, with outliers, with the PowerStic-CC_100 Po/SSC IC Inserted average being 277 Watts per hour per server, and the PowerStic-CC_100 PO/SSC IC Extracted average being 293 Watts per hour per server, a difference of 16 Watts per hour per server, or 5.5% in Paypal systems.

	PowerStic-CC_100 Inserted 24 Hr Average (W)	PowerStic-CC_100 Extracted 24 Hr Average (W)
	262	288
	270	292
	287	291
	291	297
Composite Average	277	293

Table 5: Server 016 (24 Hour Power Averages)

Table 5 shows the average power consumption for server 016 with the PowerStic-CC_100 PO/SSC IC inserted and extracted for each 24 hour period tested. Observing the values in the table, one sees the normal variance that is the result of data processing loads and OS activity. Individually, the values, PowerStic-CC_100 PO/SSC IC Inserted vs Extracted, seem to show a conflicted result in PowerStic-CC_100 PO/SSC IC performance. In some cases, the PowerStic-CC_100 PO/SSC IC seems to draw additional power, in other cases, less power. Averaging, however shows the true picture, and always reveals a power advantage when using the PowerStic-CC_100 PO/SSC IC in server and computer systems.

Multiplying this 16 watt PowerStic-CC_100 PO/SSC IC created difference shown in Figure 36 by 24 hrs per day and then by 30 days in a month, one arrives at 11.5 Kilowatts saved per month per server.

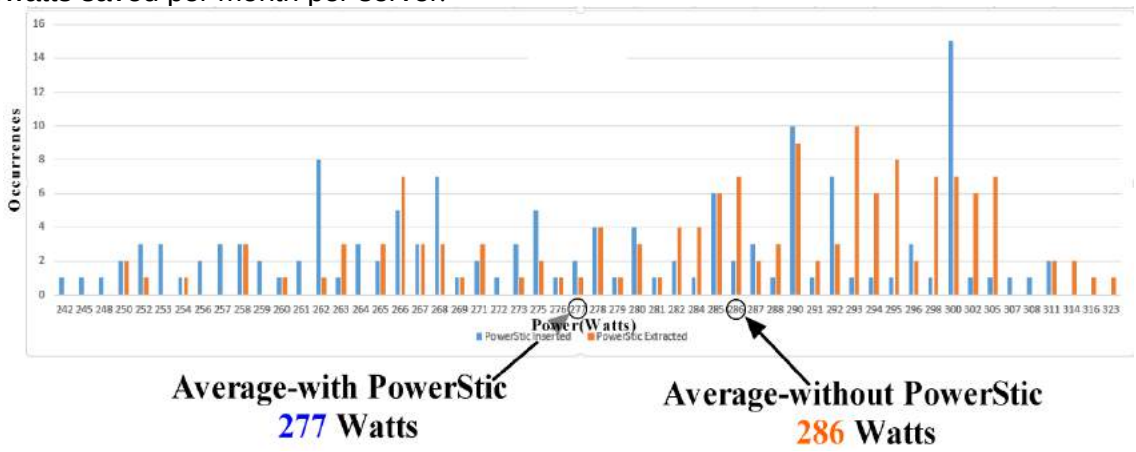


Figure 37: Server 019 Savings Composite Histogram 9 Watts/Server/Hour

Figure 37 shows a 4 day sampled composite Histogram server 019 with and without the PowerStic-CC_100 PO/SSC IC inserted in the 019 machine. The blue data (PowerStic-CC_100 PO/SSC IC Inserted) and power average shows substantially lower power than the PowerStic-CC_100 PO/SSCIC Extracted data (brown). The data shows an

approximate normal distribution, with outliers, with the PowerStic-CC_100 PO/SSC IC Inserted average being 277 Watts per hour per server, and the PowerStic-CC_100 PO/SSC IC Extracted average being 286 Watts per hour per server, a difference of 9 Watts per hour per server, or 3.1% in Paypal systems.

	PowerStic-CC_100 Inserted 24 Hr Average (W)	PowerStic-CC_100 Extracted 24 Hr Average (W)
	287	294
	290	289
	262	291
	265	266
Composite Average	277	286

Table 6: Server 019 (24 Hour Power Averages)

Table 6 shows the average power consumption for server 019 with the PowerStic-CC_100 PO/SSC IC inserted and extracted for each 24 hour period tested. Observing the values in the table, one sees the normal variance that is the result of data processing loads and OS activity. Individually, the values, PowerStic-PO/SSC IC Inserted vs Extracted, seem to show a conflicted result in PowerStic-CC_100 PO/SSC IC performance. In some cases, the PowerStic-CC_100 PO/SSC IC seems to draw additional power, in other cases, less power. Averaging, however shows the true picture, and always reveals a power advantage when using the PowerStic-CC_100 PO/SSC IC in server and computer systems.

Multiplying this 9 watt PowerStic-CC_100 PO/SSC IC created difference, shown in Figure 37, by 24 hrs per day and then by 30 days in a month, one arrives at 6.5 Kilowatts saved per month per server.

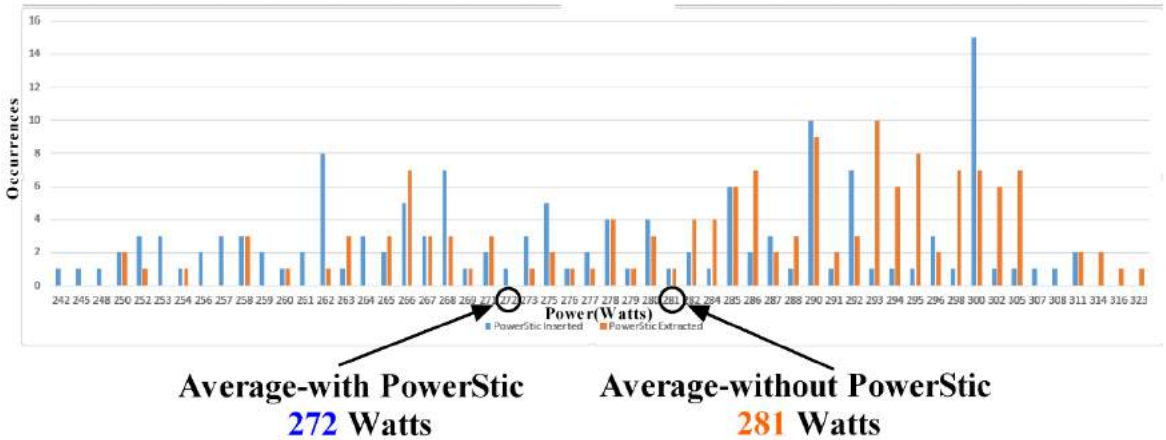


Figure 38: Server 020 Savings Composite Histogram 9 Watts/Server/Hour

Figure 38 shows a 4 day sampled composite Histogram of server 020 with and without the PowerStic-CC_100 PO/SSC IC inserted in the 020 machine. The blue data (PowerStic-CC_100 PO/SSC IC Inserted) and power average shows substantially lower power than the PowerStic-CC_100 PO/SSC IC Extracted data (brown). The data shows an approximate normal distribution, with outliers, with the PowerStic-CC_100 PO/SSC IC Inserted average being 272 Watts per hour per server, and the PowerStic-CC_100 PO/SSC IC Extracted average being 281 Watts per hour per server, a difference of 9 Watts per hour per server, or 3.2% in Paypal systems.

	PowerStic-CC_100 Inserted 24 Hr Average (W)	**PowerStic-CC_100 Extracted 24 Hr Average (W)**
	269	295
	267	272
	275	276
	279	280
Composite Average	272	281

Table 7: Server 020 (24 Hour Power Averages)

Table 7 shows the average power consumption for server 020 with the PowerStic-CC_100 PO/SSC IC inserted and extracted for each 24 hour period tested. Observing the values in the table, one sees the normal variance that is the result of data processing loads and OS activity. Individually, the values of PowerStic-CC_100 PO/SSC IC Inserted vs Extracted, seem to show a conflicted result in PowerStic-CC_100 PO/SSC IC performance. In some cases, the PowerStic-CC_100 PO/SSC IC seems to draw additional power, in other cases, less power. Averaging, however shows the true picture, and always reveals a power advantage when using the PowerStic-CC_100 PO/SSC IC in server and computer systems.

Multiplying this 9 watt PowerStic created difference, shown in Figure 37, by 24 hrs per day and then by 30 days in a month, one arrives at 6.5 Kilowatts saved per month per server

Caveat on Power Types

It is well known that digitally generated power losses in any system are directly proportional to the digital activity in said system. It should be noted that power drawn by any system is a mixture of constant DC and average, dynamic or “rms” ac derived power. The presence of these two power loads result in a “power mixture ratio” consisting of an AC generated portion and a constant DC generated portion. This

“power mixture ratio” varies system to system, driven by the types of circuits utilized in a given system.

The CC-100 is sensitive and reacts to only the average, dynamic or “rms” ac derived power present in a given system. It can do nothing to reduce constant DC power. Therefore, the effectiveness of the CC-100 in reducing power will be greatly influenced by the type of circuits used in a given system.

If the system power draw is a large percentage constant DC, this will reduce the amount of power the CC-100 can recycle and save. In a pure constant DC system, the amount of power the CC-100 could potentially save could be zero.

If on the other hand, the system is primarily or completely digital and the system power draw is primarily average dynamic or “rms” ac derived power, the CC-100 power savings could be close to the 20% factor described in this datasheet.

Designers should be aware of the above realities and attempt to assess the “power mixture ratio” of their systems when evaluating the CC-100.

CC-100 PO/SSC IP Availability

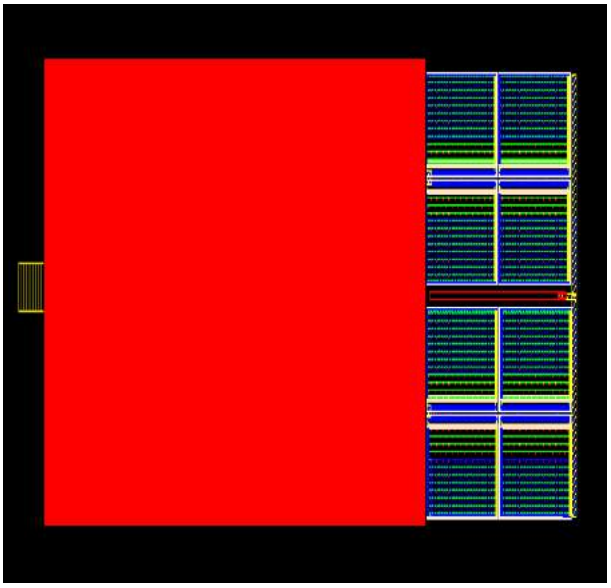
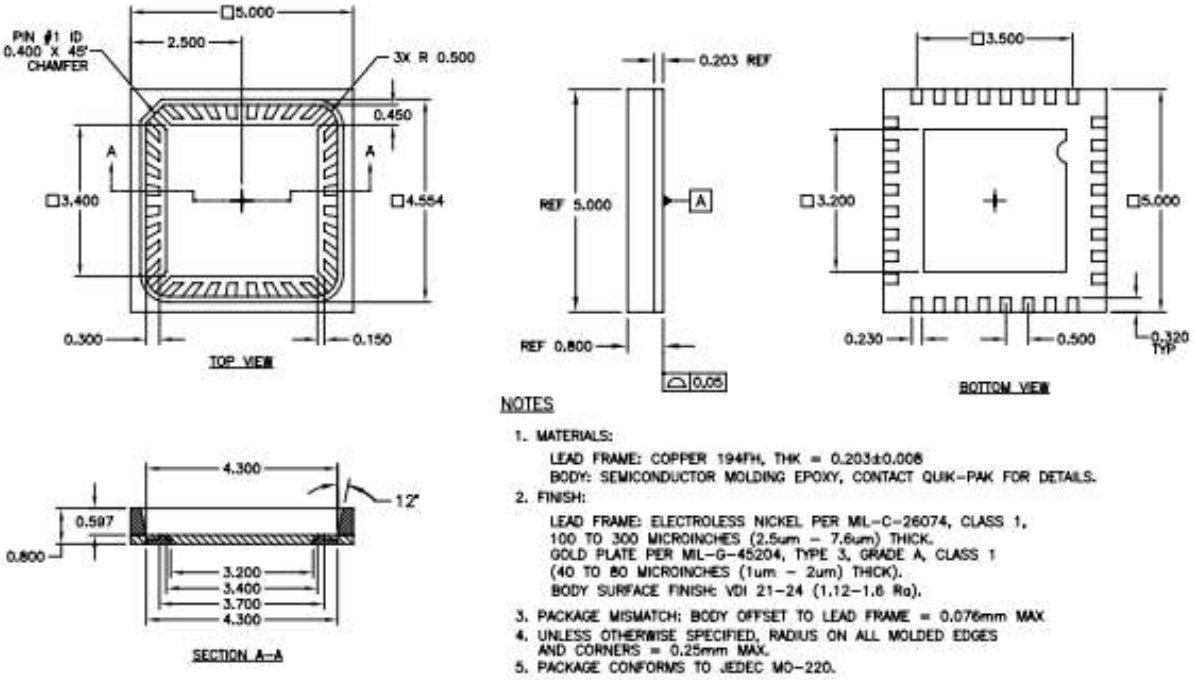


Figure 39: CC-100 PO/SSC IP-Form of a DCAP

The CC-100 Power Optimizer IC is available in IP format. Presently being produced on IBM .18um technology, the core design is easily ported to any modern CMOS process. The CC-100 Evaluation Board/Reference Design makes an easy demonstration of this technology.

The CC-100 Evaluation Board/Reference Design is available for a nominal fee from CurrentRF. Contact Michael.Hopkins@CurrentRF.com for more details or information.

Packaging Information



NOTES

1. MATERIALS:
   LEAD FRAME: COPPER 194FH, THK = 0.203±0.008
   BODY: SEMICONDUCTOR MOLDING EPOXY, CONTACT QUIK-PAK FOR DETAILS.
2. FINISH:
   LEAD FRAME: ELECTROLESS NICKEL PER MIL-C-26074, CLASS 1,
   100 TO 300 MICROINCHES (2.5um - 7.6um) THICK.
   GOLD PLATE PER MIL-G-45204, TYPE 3, GRADE A, CLASS 1
   (40 TO 80 MICROINCHES (1um - 2um) THICK).
   BODY SURFACE FINISH: VDI 21-24 (1.12-1.6 Ra).
3. PACKAGE MISMATCH: BODY OFFSET TO LEAD FRAME = 0.076mm MAX
4. UNLESS OTHERWISE SPECIFIED, RADIUS ON ALL MOLDED EDGES AND CORNERS = 0.25mm MAX.
5. PACKAGE CONFORMS TO JEDEC MO-220.

Contact Information:

For additional technical or ordering information contact us at:

8558 Maul Oak Drive

West Jordan, Utah 84081

www.CurrentRF.com

(209)-914-2305

Michael.Hopkins@CurrentRF.com

Voltage Regulator Addendum

Voltage regulator manufacturers specify their devices in terms of forward transfer (S21) or, unregulated input to regulated output performance characteristics. Little to nothing is defined in terms of reverse regulator isolation, or S-parameter S12. Further, there is very little regulator performance information at frequencies above and beyond 10 MHz, in the forward or reverse direction.

Is it of any importance how well voltage regulators isolate activity occurring at their outputs from their inputs? Generally, this subject has been considered "leakage" in the system, and has not been studied. With the advent and production of the CurrentRF PowerStic and Exodus devices, it has been discovered that capturing and harnessing this leakage can be a source of considerable harvested power.

This paper presents measured data gathered on linear and switch mode regulators with respect to broadband reverse regulator isolation. Regulator manufacturer data sheet information is examined in light of device measured reverse isolation, and collected data is correlated to the published data found in regulator manufacturer datasheets.

Linear Regulators

Although there is a plethora of linear voltage regulator designs in today's marketplace on a variety of processes, one can roughly categorize them into two very broad categories, series pass and low drop out (LDO).

Linear Series Pass Linear Regulators

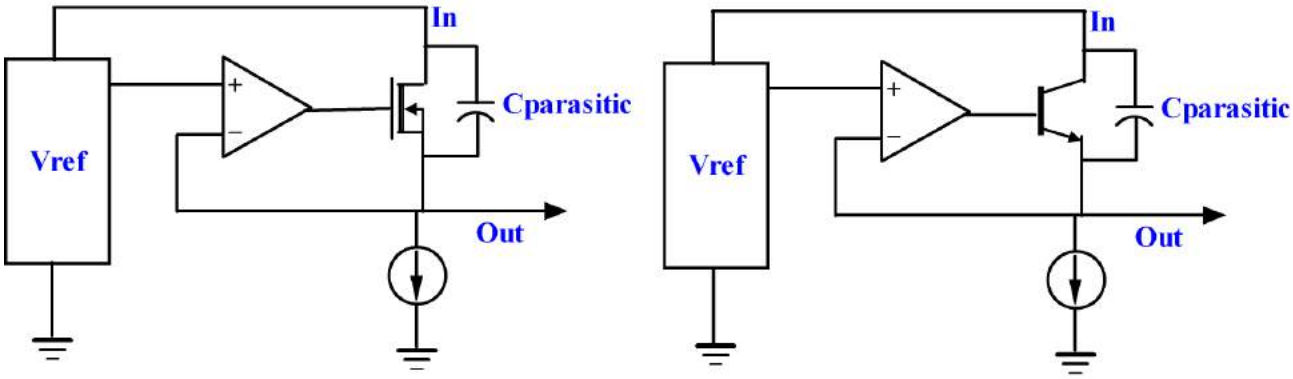


Figure 1: Linear Series Pass Regulator Architecture

Figure 1 shows the basic architecture of a linear series pass regulator. Generally, the regulator consists of a fixed reference (Vref) and a Fet or a bipolar transistor controlled and driven by a negative feedback loop containing a high gain element (Op Amp). Usually, a current source is utilized to bias the series pass element in the architecture, but can be omitted in low power applications. The Cparasitic element in the above architecture is generally ignored in most applications, but is important when considering the effects of high frequency reverse isolation in regulators.

Basic Models

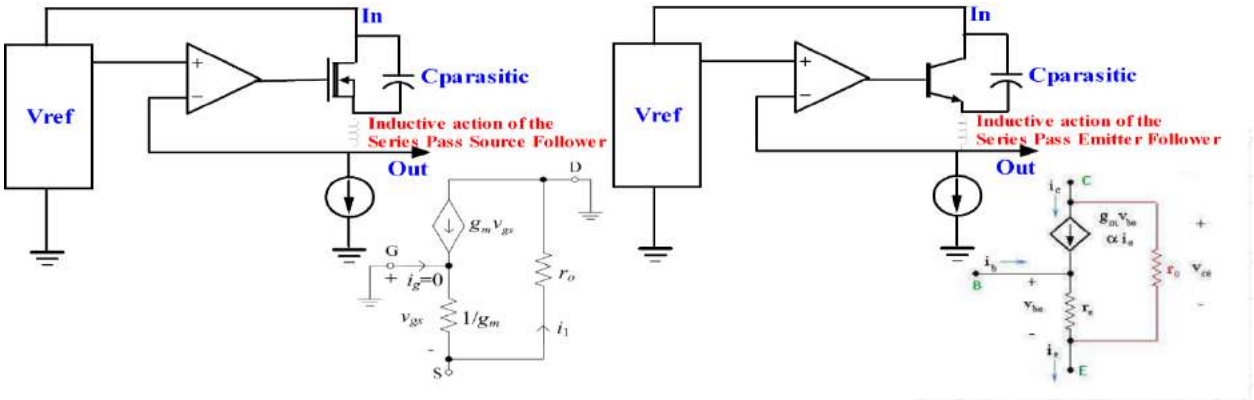


Figure 2: Linear Series Pass Regulator Models

The series pass element in the architectures shown in Figures 1 and 2 determine the high frequency reverse isolation characteristics of the series pass regulator. Small signal hybrid T modeling is appropriate for use here, in that the small signal dynamic characteristics of the series pass transistor set the reverse isolation performance of the regulator in this configuration. The series pass architecture has an inductive characteristic (see figures 2 and 3) due to the embedded emitter/source follower transistor configuration. At DC or frequencies at or below the unity gain bandwidth of the control Op Amp, the control loop forces the gate/base of the series pass transistor to track the events at the source/emitter, thus cancelling the follower inductive effect. At frequencies above the unity gain bandwidth of the control Op Amp, however, the series pass element in the architecture is free to react to current changes through the series pass transistor, acting much like an embedded inductor in series with the transistor source/emitter and the output node of the regulator.

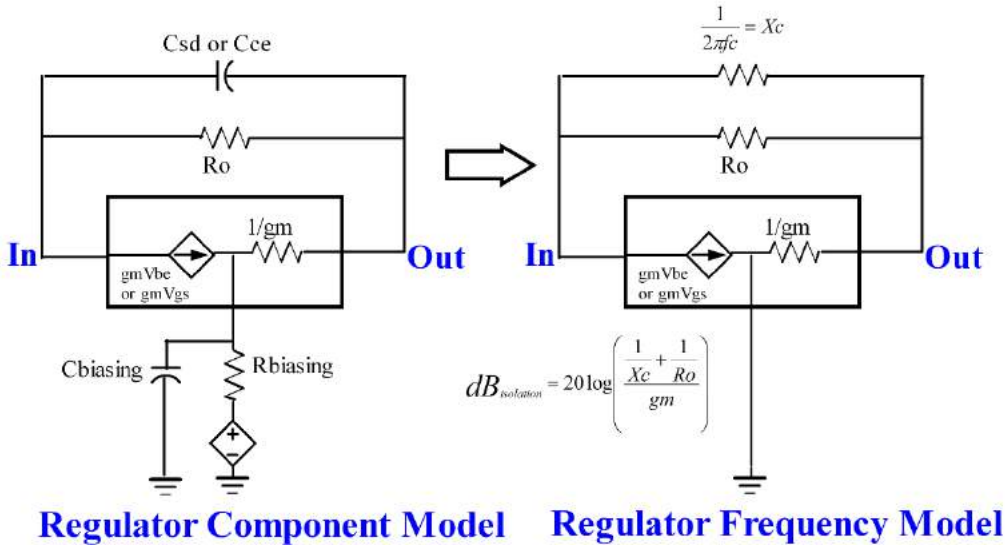
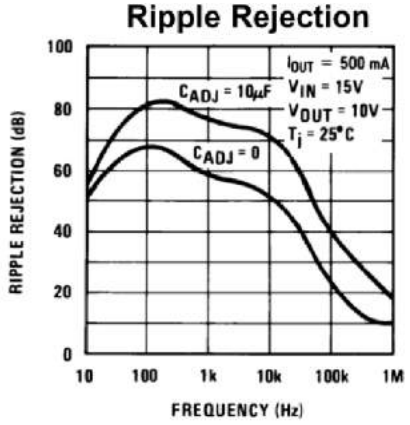


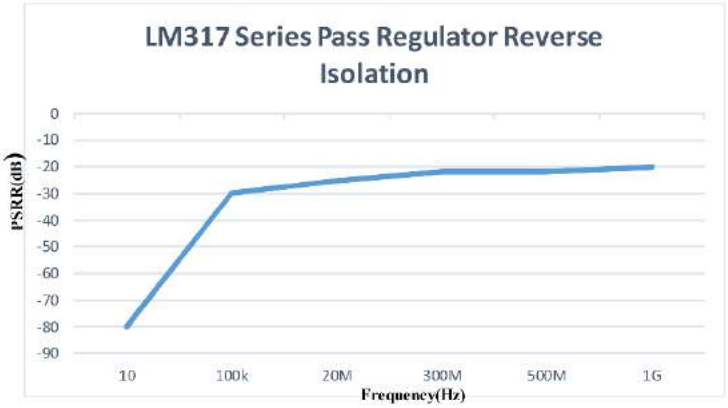
Figure 3: Linear Series Pass Regulator Macro Model

The simplified models of Figure 3 show the elements involved and the mathematical relationship as it relates to regulator reverse isolation. The model shown in Figure 3 shows a simple high frequency relationship between the output resistance of the series pass element (Ro), the frequency response of the bridging capacitance (Xc), and the gm of the series pass element in the architecture. The result is the reverse isolation of the regulator, expressed in dB.

Referring to Figure 3, as Xc or gm of the device increases, the reverse isolation of the regulator increases. Thus at relatively low noise frequencies, Xc, the reactance of the bridging capacitor, increases, lowering the overall conductance, forcing currents through the series pass device, changing the gm, changing the device Vgs /Vbe, causing the device's inductive effect. As frequencies increase, Xc decreases, increasing the bridging conductance, decreasing the device gm change, thus decreasing the series pass device inductive effect. As frequencies increase further, the Xc of the bridging capacitance becomes low enough so as to compete with the 1/gm input resistance of the series pass device, thus further decreasing the inductive effect of the of the series pass device. This "break point" can be adjusted by either increasing the bridging capacitance value, or increasing the DC current through the regulator series pass device, thus increasing its gm.

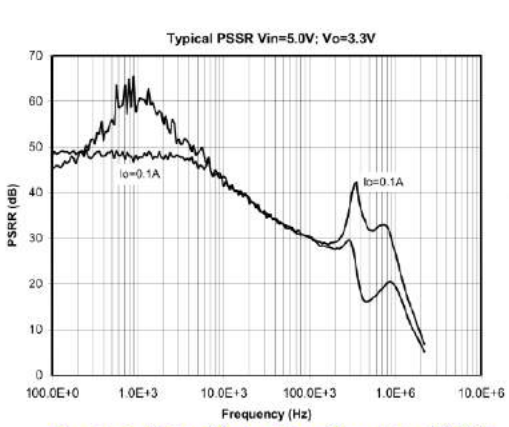


LM317 Series Pass Regulator PSRR

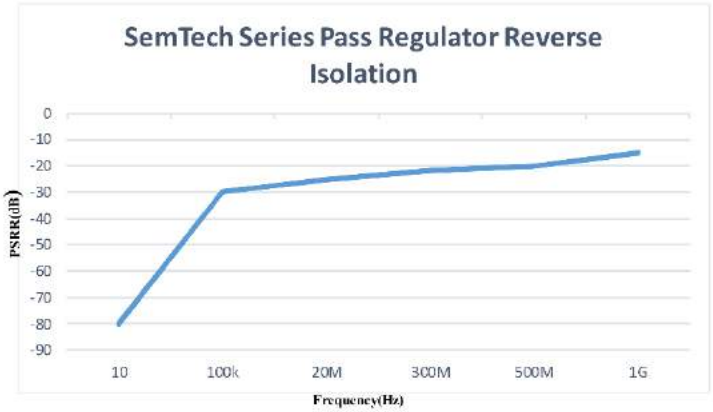


LM317 Series Pass Regulator Measured Reverse Isolation

Figure 4: National LM317 PSRR and Reverse Isolation



Semtech Native Series Pass Regulator PSRR



Semtech Native Series Pass Regulator Measured Reverse Isolation

Figure 5: Semtech SC4215A PSRR and Reverse Isolation

These effects are graphically displayed in in Figures 4 and 5. Two series pass regulators, the National LM317 and Semtech SC4215A (schematics and block diagrams shown in Figures 6 and 7) are shown to have excellent PSRR (reverse isolation) out to about 1 MHz. The PSRR/Reverse Isolation starts to degrade at frequencies greater than 1 MHz, ranging between -30dB at 1 MHz to -10dB at 1 GHz. The bipolar LM317 seems to have better isolation at 1 GHz (-20dB) than the Semtech SC4215A Native NFET Regulator (-10dB). This decrease in the Semtech Regulator reverse isolation performance is expected due to the increased bridging capacitance and lower gm of the Native MOSFET device in the SC4215A when compared to the NPN bipolar device in the LM317 Regulator.

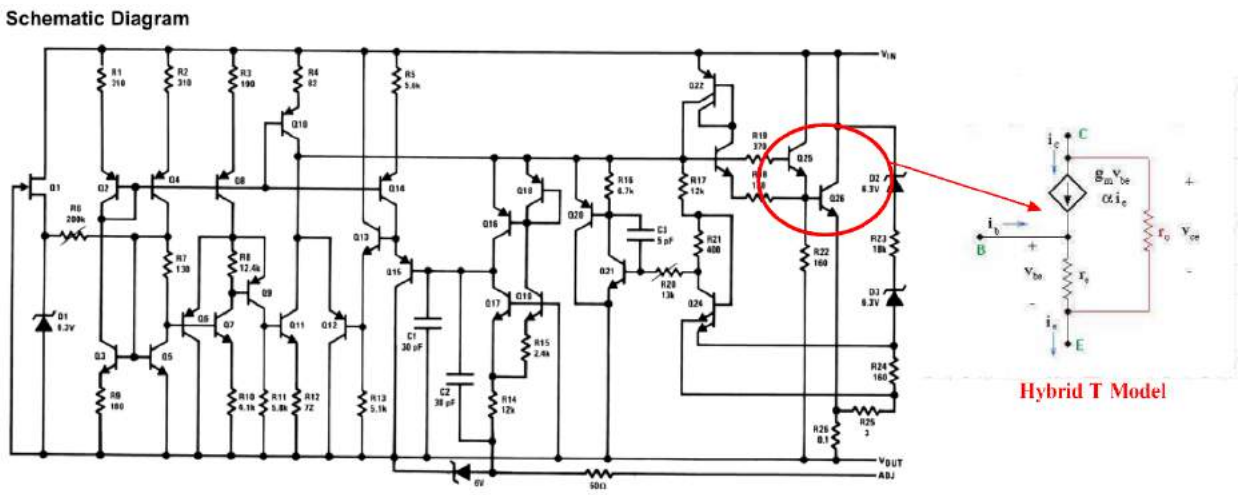


Figure 6: LM317 Series Pass Regulator

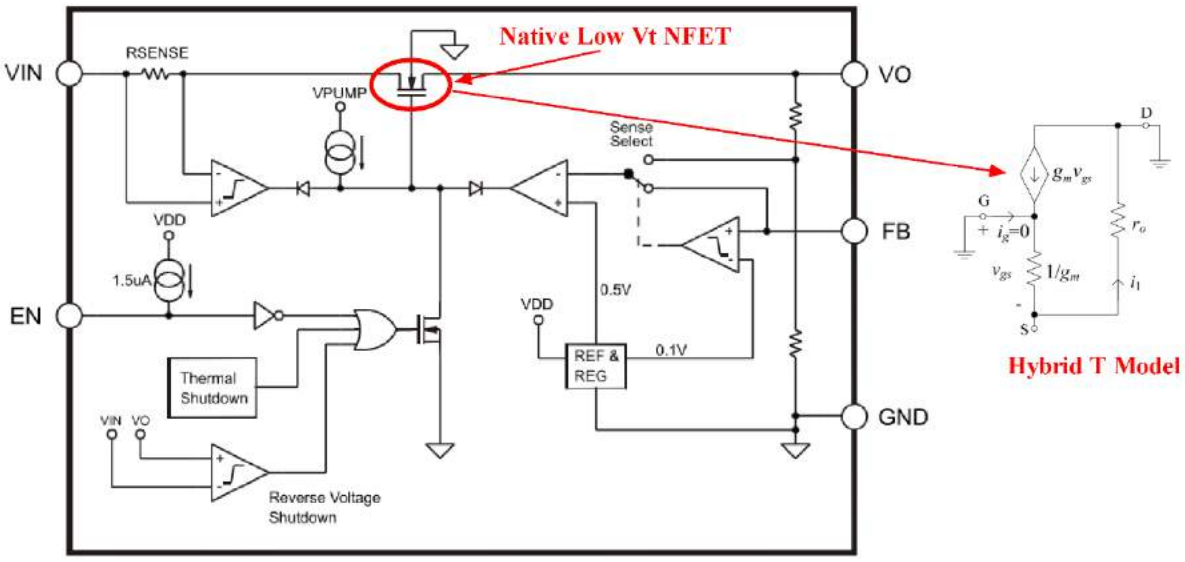


Figure 7: SemTech SC4215A Series Pass Native NFET Regulator

Figures 8, 9, and 10 show measurement results consisting of time domain supply noise and the resultant reverse coupling through the LM317 and SC4215A regulators. The noise source is a Pseudo-Random Linear

Feedback Shift Register (LSFR) which produces a cyclical, repeatable noise pattern for testing. Figures 8 and 9 show the simplified top level test structures, Figure 10 shows close-ups and measurement results of the resultant input waveform when the regulator is required to supply dynamic currents to the LSFR without the aid of a reservoir capacitor. In observing the LM317/SC4215A regulator input waveform, one can clearly see much reduced frequency content on the input waveform verses what is being required of the regulator by the LSFR. Since the impedances at the input supply and output nodes of the regulators are similar, one can conclude that the inductive action of current being pulled from the series pass regulators is tracking and supplying the needed dynamic currents, leaving only small amounts of AC residuals and DC tracking currents at the regulator input supply node.

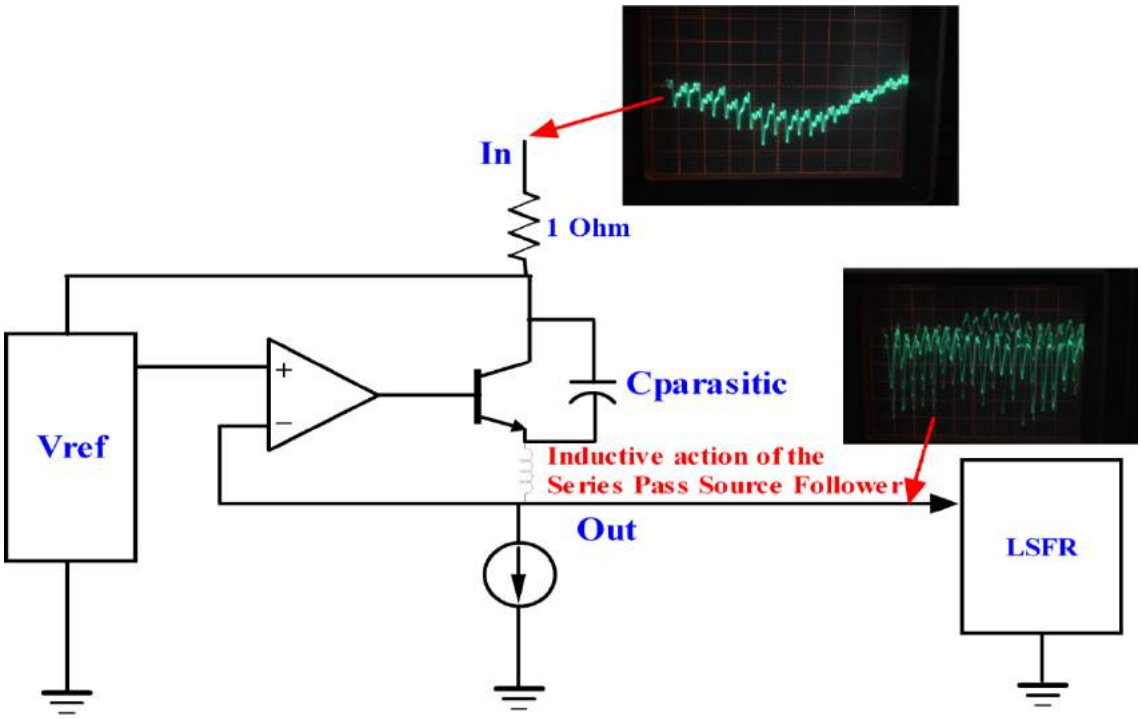


Figure 8: LM317 Series Pass Regulator Reverse Isolation Test

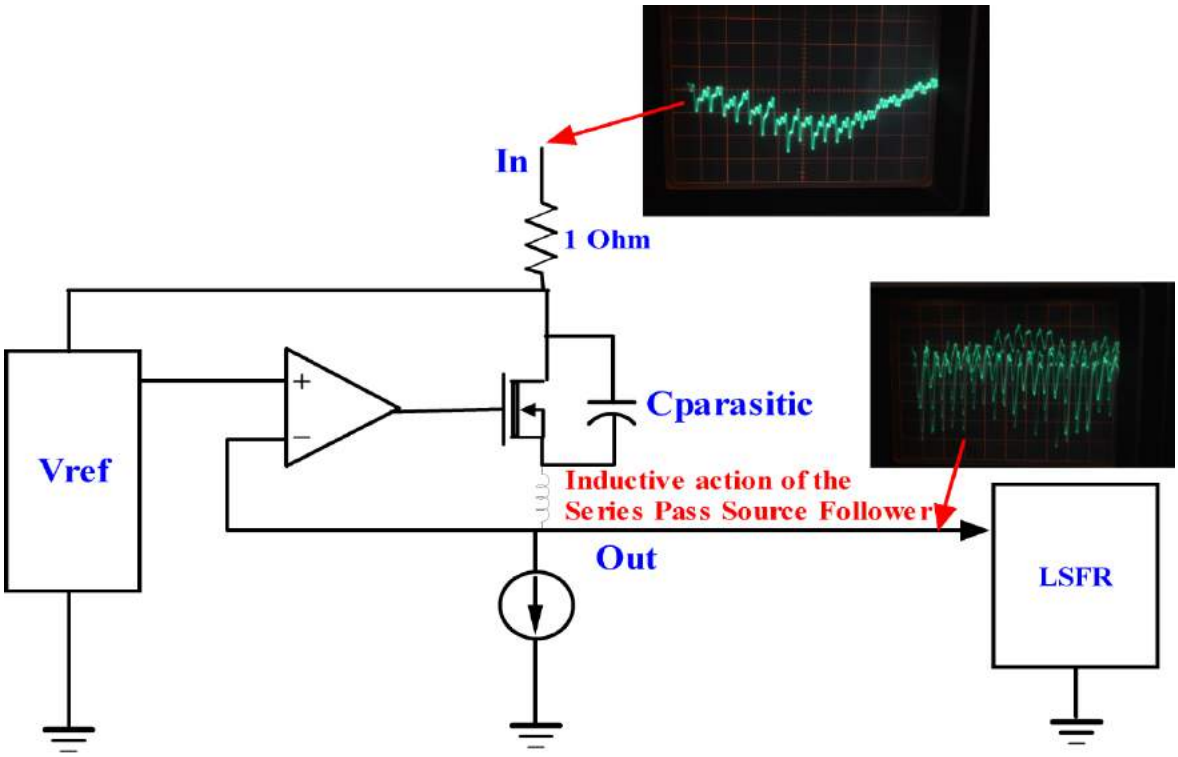
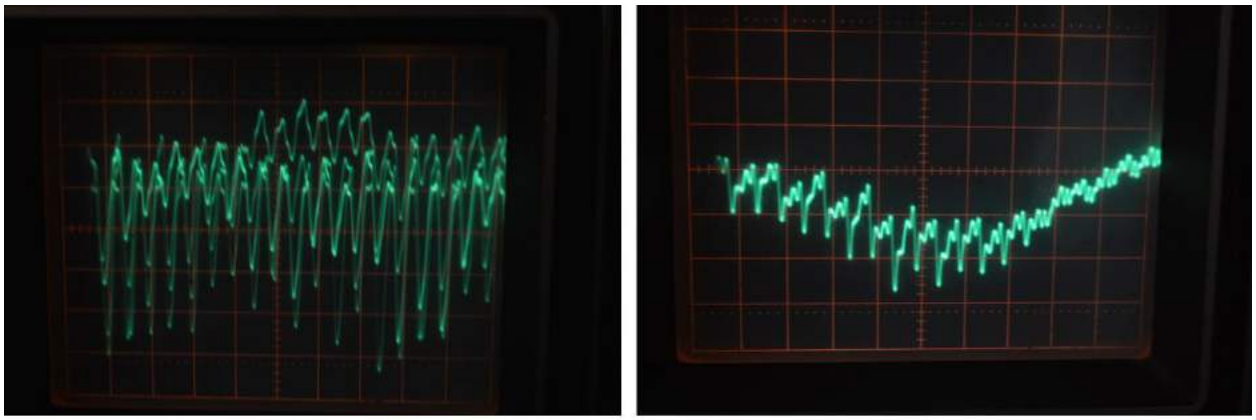


Figure 9: SC4215A Series Pass Native NFET Regulator Reverse Isolation Test



Regulator Ouptut--50mV per Division
(200mVpp Supply Noise)

Regulator Input--20mV per Division
(30mVpp max Noise Leakage)

Figure 10: Series Pass Regulator Reverse Isolation Performance

The Figure 8, 9, and 10 test shows the inherent isolation that series pass regulators provide for system internal power grids. The series pass regulator "contains" system dynamic noise and enhances the CC-100, PowerStic, and Exodus power recycling and power performance at the output node of series pass regulators.

Linear LDO Regulators

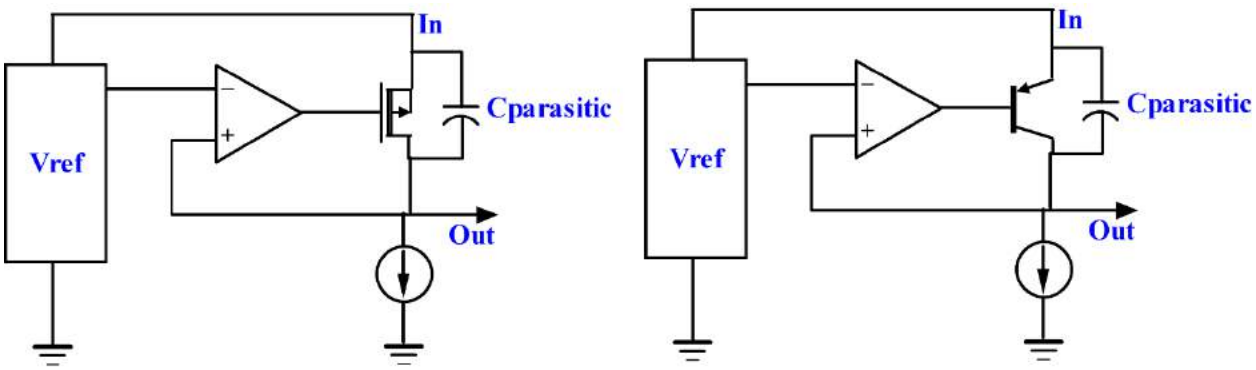


Figure 11: Linear LDO Architecture

Figure 11 shows the basic architecture of a linear low drop-out (LDO) regulator. Generally, the regulator consists of a fixed reference (Vref) and a Fet or a bipolar transistor controlled and driven by a negative feedback loop containing a high gain element (Op Amp). Usually, a current source is utilized to bias the common source element in the architecture, but can be omitted in low power applications. The Cparasitic element in the above architecture is generally ignored in most applications, but is important when considering the effects of high frequency reverse isolation in regulators

Basic Models

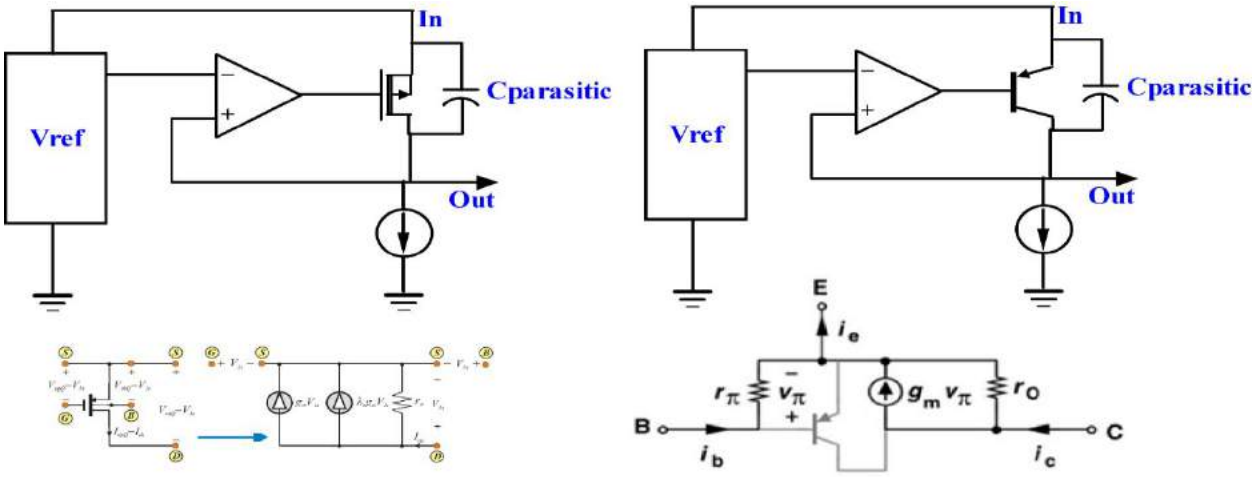


Figure 12: Linear LDO Regulator Models

The common source element in the architectures shown in Figures 11 and 12 determine the high frequency reverse isolation characteristics of the LDO regulator. Small signal hybrid pi modeling is appropriate for use here, in

that the small signal dynamic characteristics of the common source transistor sets the reverse isolation performance of the regulator in this configuration. The LDO architecture does not have an inductive characteristic (see figures 12 and 13) due to the embedded common source transistor configuration. At DC or frequencies at or below the unity gain bandwidth of the control Op Amp, the control loop forces the gate/base of the common source transistor to track the events at the drain/collector, thus enabling circuit regulation. At frequencies above the unity gain bandwidth of the control Op Amp, however, the regulator control loop cannot drive the common source element in the architecture fast enough to react to the current changes demanded of the regulator, thus Cds or Cce is the only source of the needed high frequency current.

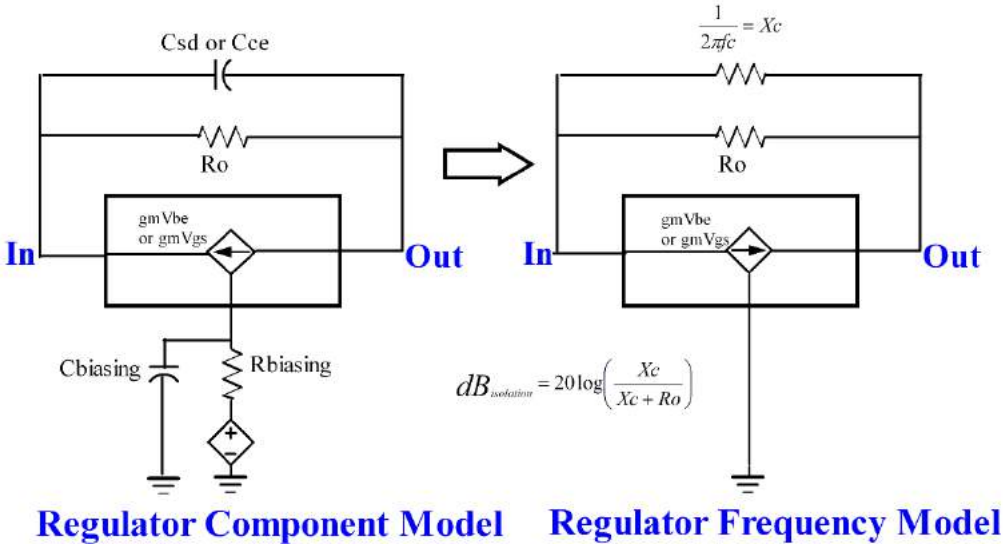
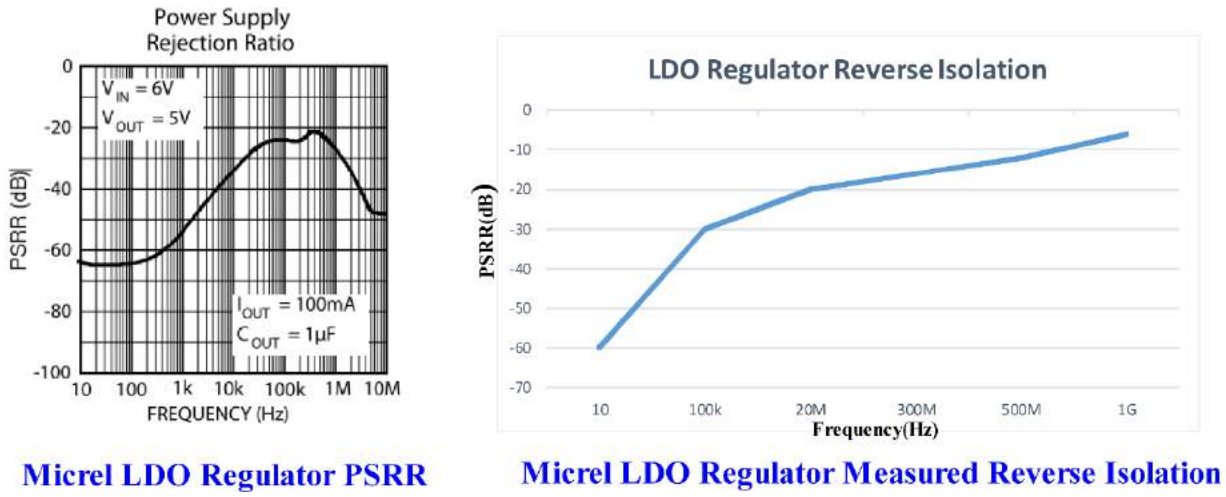


Figure 13: Linear LDO Regulator Macro Model

The simplified models of Figure 13 show the elements involved and the mathematical relationship as it relates to regulator reverse isolation. The model shown in Figure 13 shows a simple high frequency relationship between the output resistance of the series pass element (Ro) and the frequency response of the bridging capacitance (Xc), the isolation of the regulator. The resulting regulator isolation is expressed in dB.

As Xc of the bridging device increases, the reverse isolation of the regulator increases. Thus at relatively low noise frequencies, Xc, the

reactance of the bridging capacitor, increases, lowering the overall conductance, forcing currents through the common source element, forcing the control loop to drive the base/gate of the common source element to deliver the needed current to the regulator load . As frequencies increase, however, the bandwidth limited control loop cannot respond fast enough to drive the circuit common source element, Xc is seen to decrease, increasing the bridging capacitance conductance, the effect being the lowering the overall regulator reverse isolation. As frequencies increase further, the Xc of the bridging capacitance becomes low enough so as to compete with the output resistance, Ro, of the common source device, thus further decreasing the reverse isolation of the regulator. This "break point" can only be adjusted by either increasing or lowering the bridging capacitance value or increasing the control loop bandwidth. The LDO has no effective inductive reactance, thus allowing high frequency dynamic current demands to be drawn through the bridging capacitance from the regulator supply input.



Micrel LDO Regulator PSRR

Micrel LDO Regulator Measured Reverse Isolation

Figure 14: Micrel MIC5219 PSRR and Reverse Isolation

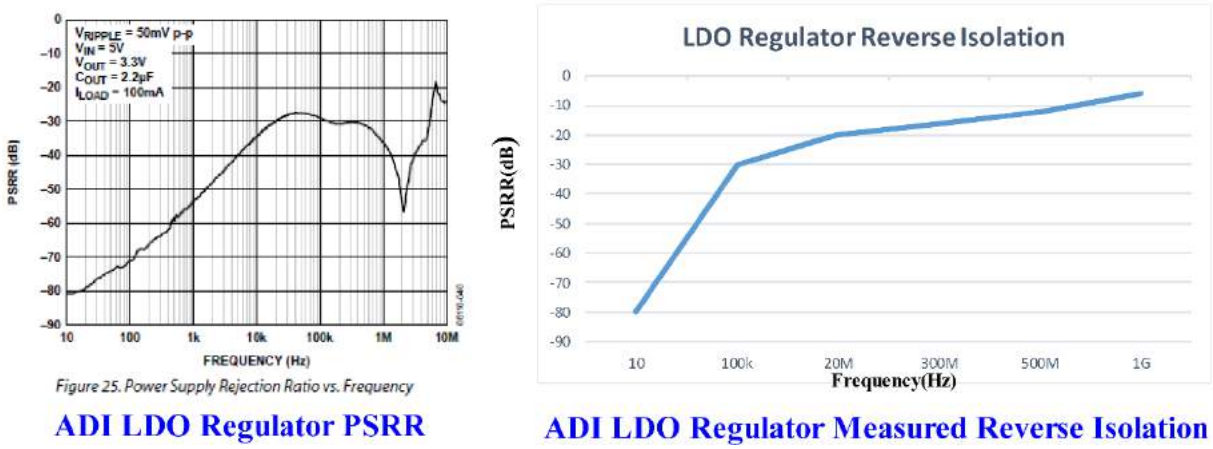
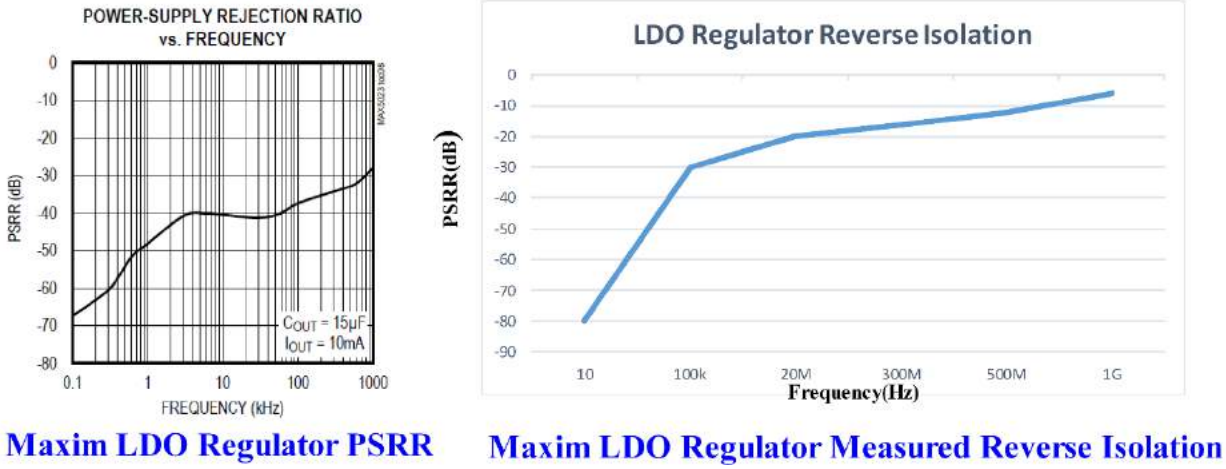


Figure 25. Power Supply Rejection Ratio vs. Frequency

ADI LDO Regulator PSRR **ADI LDO Regulator Measured Reverse Isolation**

Figure 15: ADI ADP1715 PSRR and Reverse Isolation



Maxim LDO Regulator PSRR **Maxim LDO Regulator Measured Reverse Isolation**

Figure 16: Maxim MAX5024L PSRR and Reverse Isolation

These coupling effects are graphically displayed in in Figures 14, 15, and 16. Three LDO regulators, the Micrel MIC5219, ADI ADP1715, and Maxim MAX5024L (schematics and block diagrams shown in Figures 17, 18, and 19) are shown to have excellent PSRR (reverse isolation) out to

about 1 MHz. The PSRR/Reverse Isolation starts to degrade at frequencies greater than 1 MHz, ranging between -30dB at 1 MHz to -5dB at 1 GHz.

This decrease in regulator reverse isolation performance is expected due to the decreased bridging capacitance reactance, Xc, the limited bandwidth of the control loop, and the lack of an inductive blocking element in the LDO architecture.

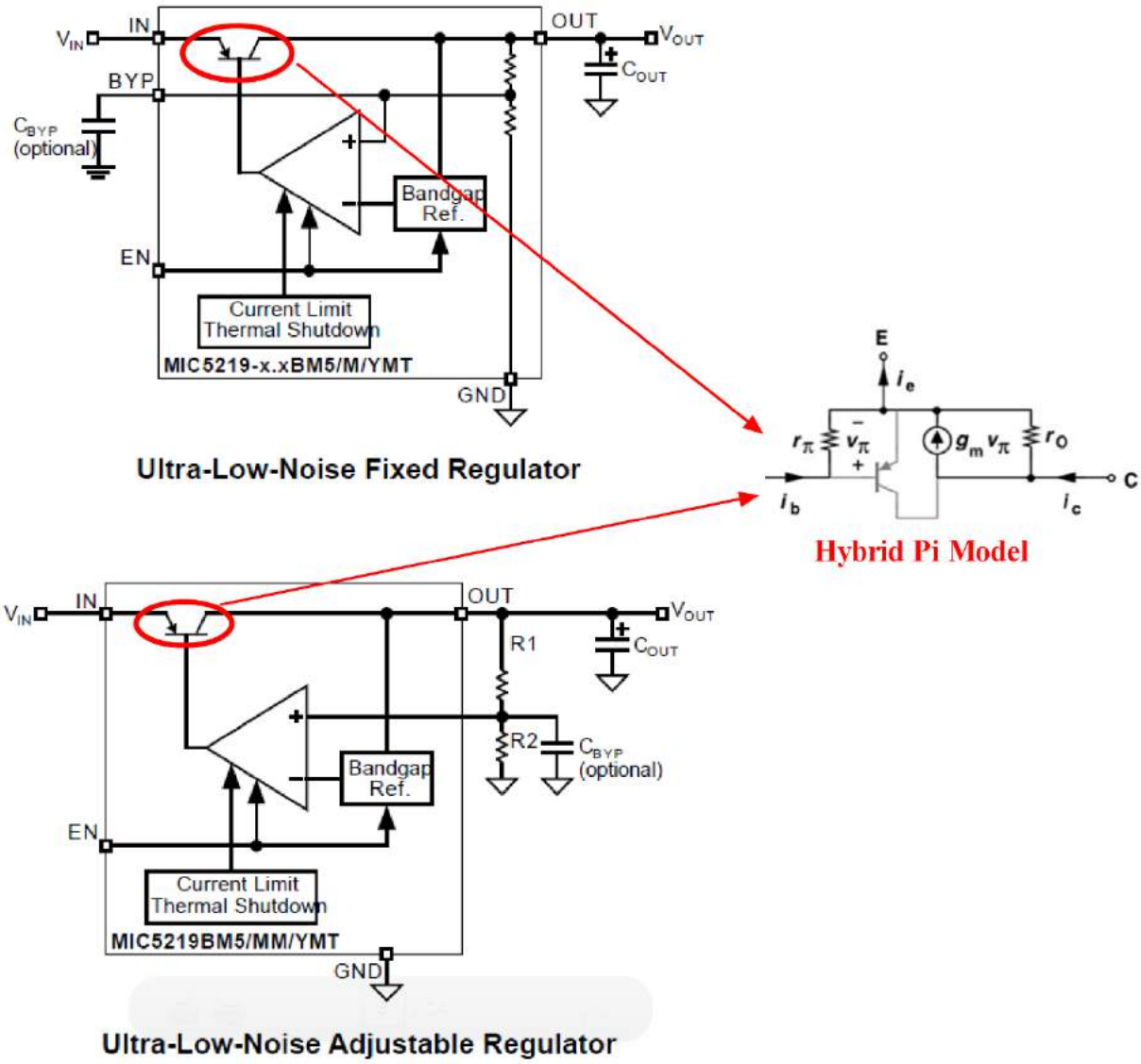


Figure 17: Micrel MIC5219 LDO Regulator

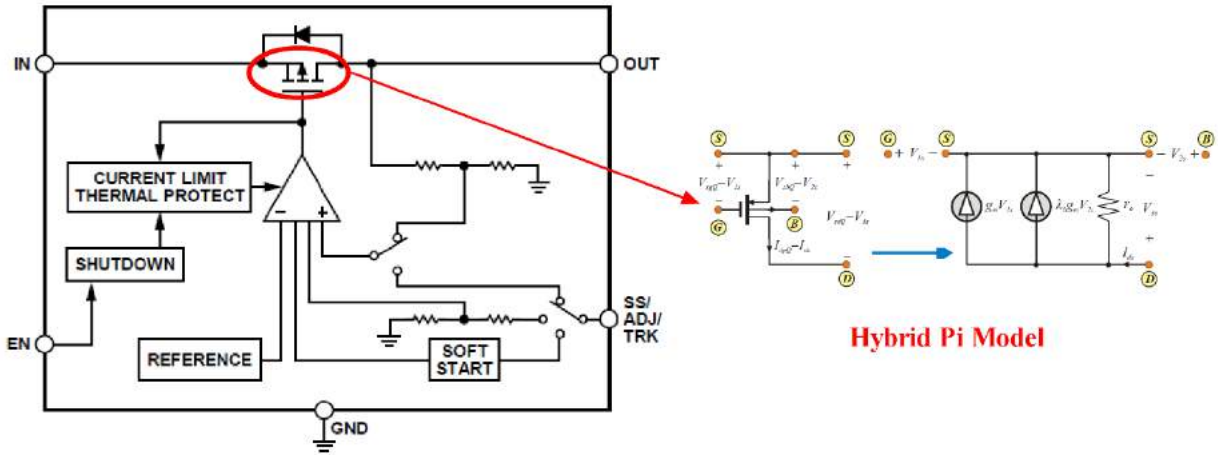


Figure 18: ADI ADP1715 LDO Regulator

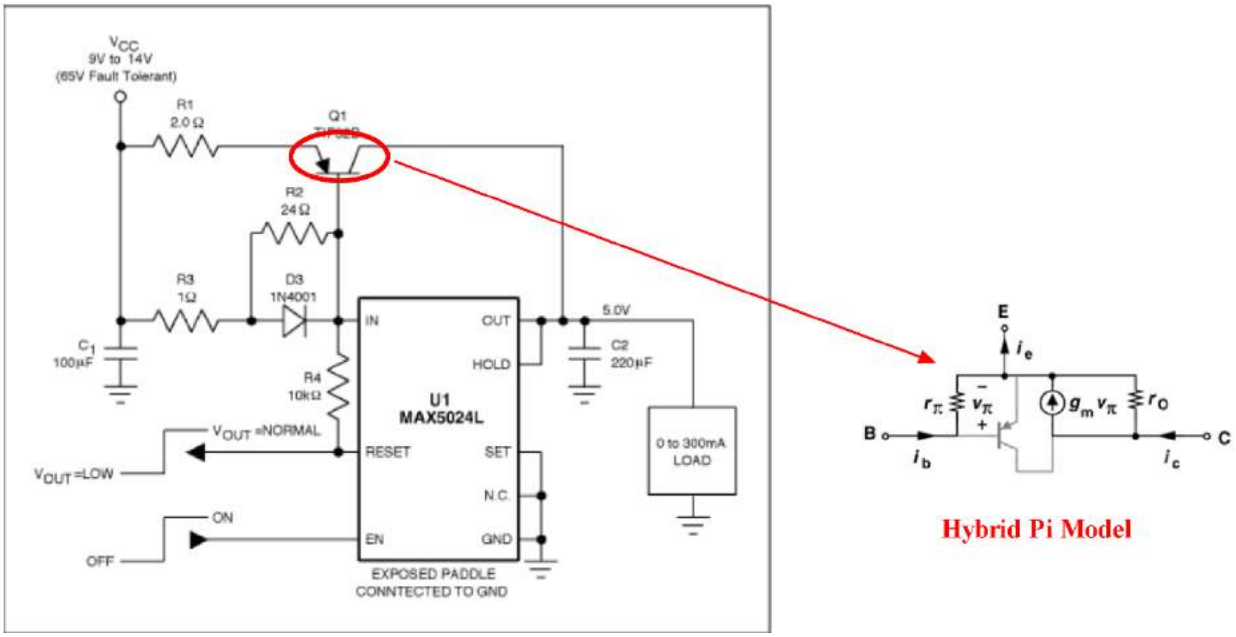


Figure 19: Maxim MAX5024L LDO Regulator

Figures 20, 21, and 22 show measurement results consisting of time domain supply noise and the resultant reverse coupling through the Micrel, ADI, and Maxim regulators. The noise source is a Pseudo-random Linear

Feedback Shift Register (LSFR) which produces a cyclical, repeatable noise pattern for testing. Figures 20 and 21 show the simplified top level test structures, Figure 22 shows close-ups and measurement results of the resultant input waveform when the regulator is required to supply dynamic currents generated by the LSFR, without the aid of an output reservoir capacitor. In observing the Micrel, ADI, and Maxim regulator input waveforms, one can clearly see a much higher magnitude and frequency content on the LDO input waveforms verses that of the LM317/Semtech regulators shown in Figure 10. Since the impedances at the input and output supply nodes of the regulators are similar, one can conclude that the high frequency dynamic currents required of the LDO cannot be obtained via the regulator circuit or common source element in the regulator, but are being drawn through the bridging capacitance around the LDO.

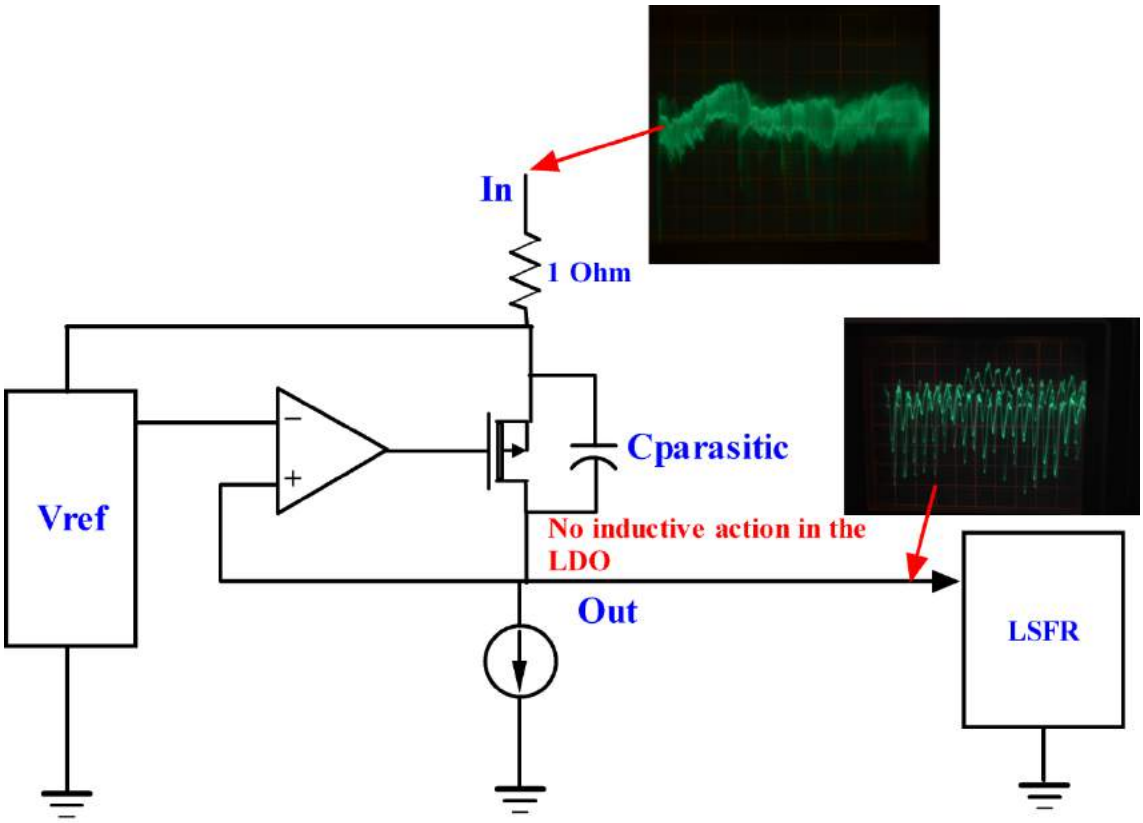


Figure 20: PMOS LDO Reverse Isolation Test

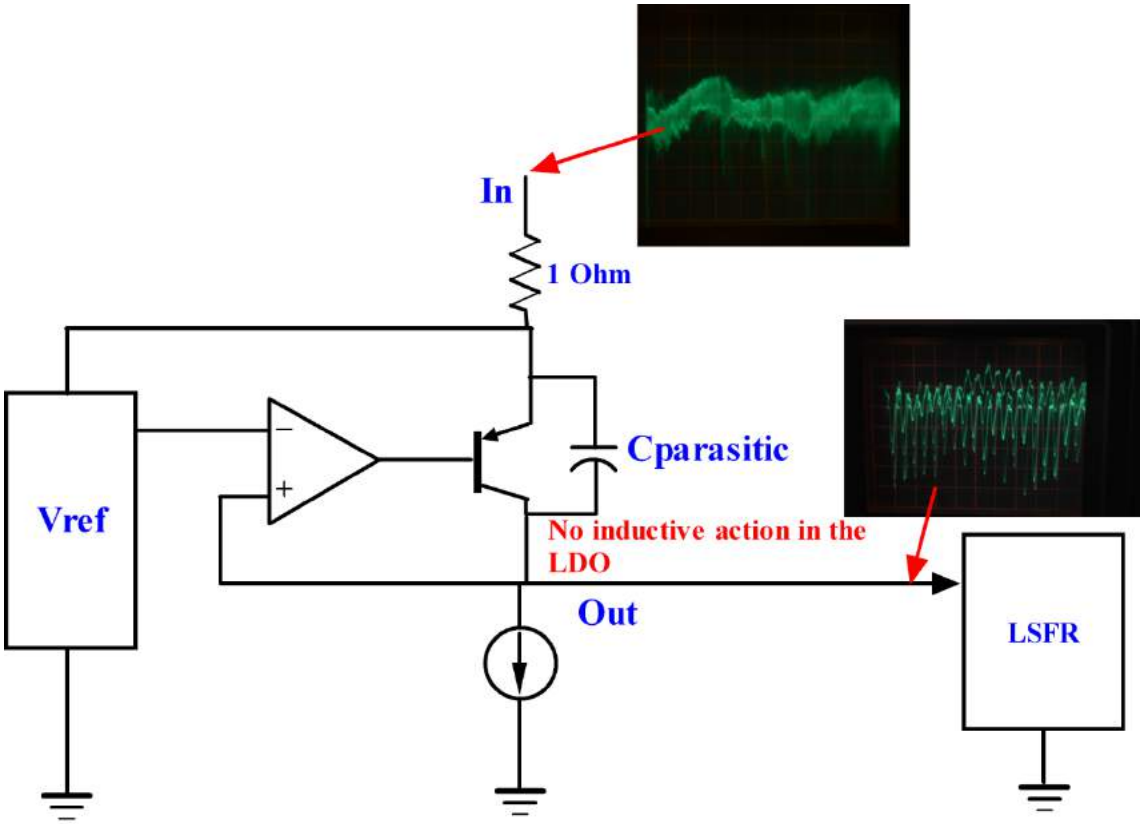
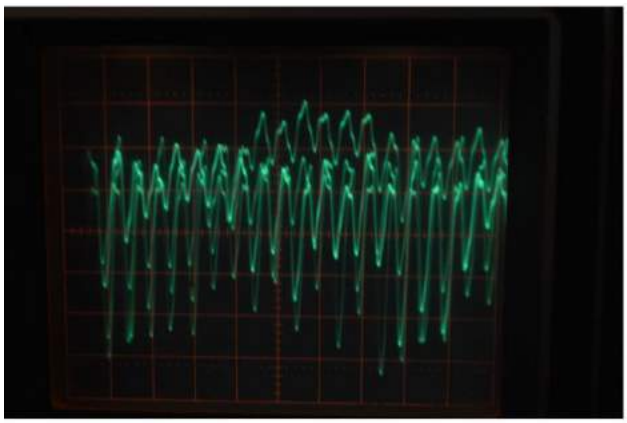
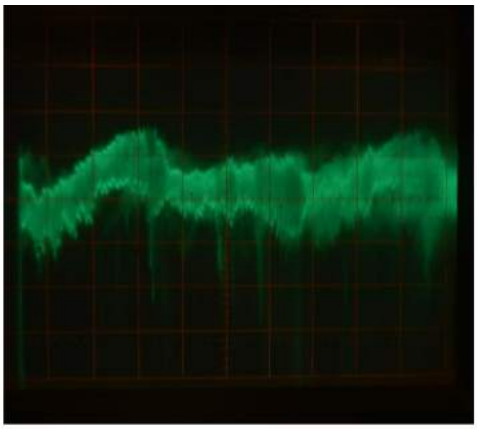


Figure 21: PNP LDO Reverse Isolation Test



Regulator Ouptut--50mV per Division (200mVpp Supply Noise)



Regulator Input--50mV per Division (100mVpp Average Noise--250mVpp High Frequency Glitches)

Figure 22: LDO Reverse Isolation Performance

The Figure 20, 21, and 22 test shows the inherently poor high frequency isolation that LDO regulators provide for system internal power grids. The LDO regulator "passes" system high frequency dynamic noise around the LDO to the output of the preceding regulator. This action explains how and why the PowerStic and Exodus devices recycle and reduce power in systems with USB ports, even if the circuit noise is not generated on the 5V USB supply.

Switch Mode Buck Regulators

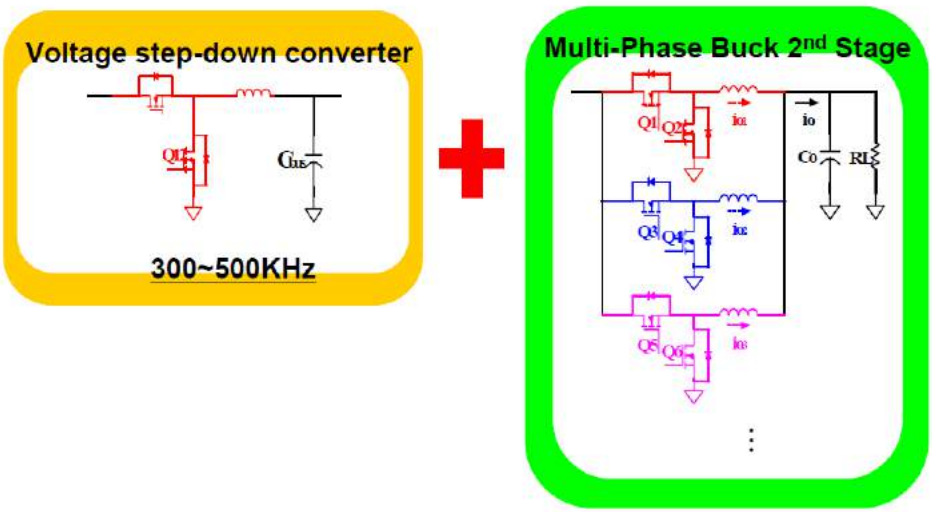


Figure 23: Typical Buck Switching Regulators

Figure 23 shows the basic topology of a switch mode Buck Converter/Regulator. A Buck Converter is a "step down" device, taking in an input high voltage and current (power), converting the input power to a lower output voltage with a "step up" in current. Buck converters are

utilized for their high efficiency in this down conversion function, and usually achieve Power In/Power Out efficiencies greater than 90%.

The Buck converter generally consists of a high power storage inductor (see Figure 24 for characteristics), an output filtering cap, a Mosfet, source connected to ground on the input of the power inductor, utilized for inductor grounding during the flyback phase of operation, and a Mosfet connected in series with the input supply, which activates during the power inductor charging or boost phase of operation.

Not much is published on the effects of high frequency noise at the output of the converter coupling back to the input of the converter and the preceding input stage, known as high frequency reverse isolation.

Features

- Available in E6 series
- Unit height of 3.8 mm
- Current up to 7.2 A
- RoHS compliant*

Applications

- Input/output of DC/DC converters
- Power supplies for:
  - Portable communication equipment
  - Camcorders
  - LCD TVs
  - Car radios

SRU1038 Series - Shielded SMD Power Inductors

Electrical Specifications

Bourns Part No.	Inductance 100 KHz (µH)	Tol. %	Q Ref.	Test Freq. (MHz)	SRF Typ. (MHz)	RDC (mΩ)	Irms Max. (A)	Isat Typ. (A)	**K-Factor
SRU1038-1R5Y	1.5	± 30	14	7.96	65.0	5.2	7.20	7.00	177
SRU1038-2R2Y	2.2	± 30	12	7.96	55.0	7.7	6.80	6.50	145
SRU1038-2R5Y	2.5	± 30	12	7.96	50.0	12.5	6.10	6.00	136
SRU1038-3R5Y	3.5	± 30	14	7.96	24.0	11.5	5.50	5.50	106
SRU1038-3R8Y	3.8	± 30	14	7.96	35.0	15.0	5.50	5.50	104
SRU1038-5R0Y	5.0	± 30	12	7.96	30.0	14.5	4.60	4.80	94
SRU1038-5R2Y	5.2	± 30	12	7.96	30.0	22.0	4.60	4.80	92
SRU1038-6R2Y	6.2	± 30	12	7.96	25.0	16.5	4.00	4.20	84
SRU1038-6R8Y	6.8	± 30	13	7.96	36.0	35.0	3.90	4.00	80
SRU1038-8R2Y	8.2	± 30	12	7.96	22.0	32.0	3.80	3.90	73
SRU1038-100Y	10.0	± 30	24	7.96	20.0	25.0	3.80	3.60	64
SRU1038-150Y	15.0	± 30	24	2.52	16.0	37.0	2.80	2.70	51
SRU1038-220Y	22.0	± 30	20	2.52	12.0	55.8	2.20	2.30	43
SRU1038-270Y	27.0	± 30	22	2.52	11.0	78.0	1.85	1.90	39
SRU1038-330Y	33.0	± 30	22	2.52	10.0	86.0	1.80	1.80	35
SRU1038-470Y	47.0	± 30	22	2.52	8.0	121.0	1.65	1.60	29
SRU1038-680Y	68.0	± 30	24	2.52	7.0	166.0	1.10	1.30	26
SRU1038-101Y	100.0	± 30	24	0.796	6.0	220.0	1.30	1.10	20
SRU1038-151Y	150.0	± 30	20	0.796	5.0	358.0	0.90	0.80	16
SRU1038-221Y	220.0	± 30	22	0.796	4.0	565.0	0.65	0.65	14
SRU1038-331Y	330.0	± 30	20	0.796	3.0	773.0	0.55	0.52	11

**K-Factor: To calculate core flux density, Bp-p (gauss) = K x L(µH) x Δ I (peak-to-peak ripple current, A), determine core loss from *Core Loss vs. Flux Density* plot on page 2.

General Specifications

Test Voltage ..... 1 V
Reflow Soldering .. 230 °C, 50 sec. max.
Operating Temperature
..... -40 °C to +125 °C
(Temperature rise included)
Storage Temperature
..... -40 °C to +125 °C
Rated Current
..... Ind. drop 35 % typ. at Isat
Temperature Rise
..... 40 °C max. at rated Irms
Resistance to Soldering Heat
..... 260 °C for 10 sec.

Materials

Core ..... Ferrite DR and RI core
Wire ..... Enameled copper
Terminal ..... Ag/Ni/Sn
Packaging ..... 800 pcs. per reel

Product Dimensions

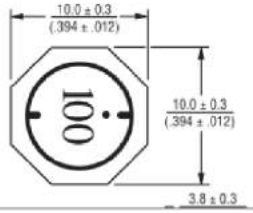


Figure 24: Buck Switching Inductor Characteristics

Figure 25 shows the basic Buck converter components and their important parasitic components. One will notice in Figure 25 and the table in Figure 24, that power inductors tend to have relatively high inductance values (uH), low self-resonant frequencies, therefore, high inter-winding capacitances. Assuming sufficient magnitude high frequency, dynamically generated, load noise, and also assuming a relatively low Q filter capacitor at the Buck Converter output, the inter-winding power inductor capacitance is high enough in value (about 8pF with the highlighted 47uH inductor of Figure 24) to provide a pass through capacitance for this noise back to the converter input.

The simplified models of Figure 25 show the converter in its boost or charging phase, with the Mosfets switched to their appropriate states, providing a low impedance path for high frequency noise passing through the power inductor, blocked by an approximated 100nh of trace inductance of the flyback path, forcing noise currents through the "on" input power Mosfet. This path on the right hand side of Figure 25 reduces to essentially a low series Mosfet channel resistance and the inter-winding power inductor capacitance.

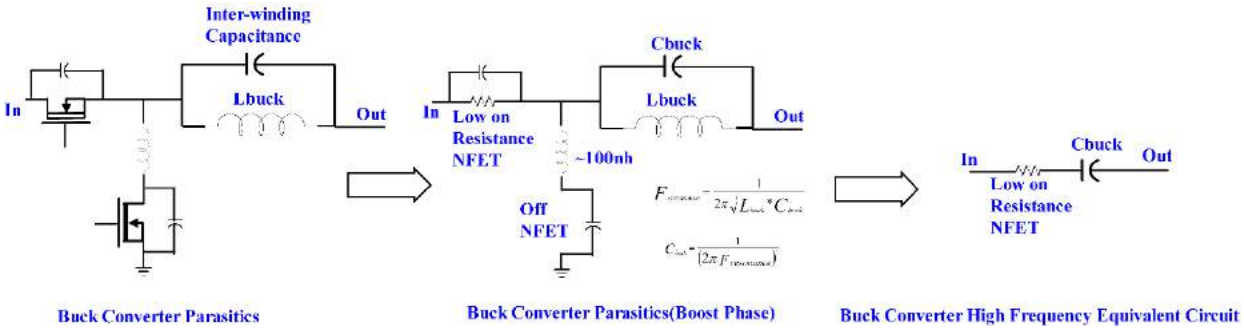


Figure 25: Buck Switching Regulator Macro Models

As Figure 25 depicts, the Buck Converter in the boost or changing phase, reduces to a simple low R, moderate C coupling circuit for high frequency load noise.