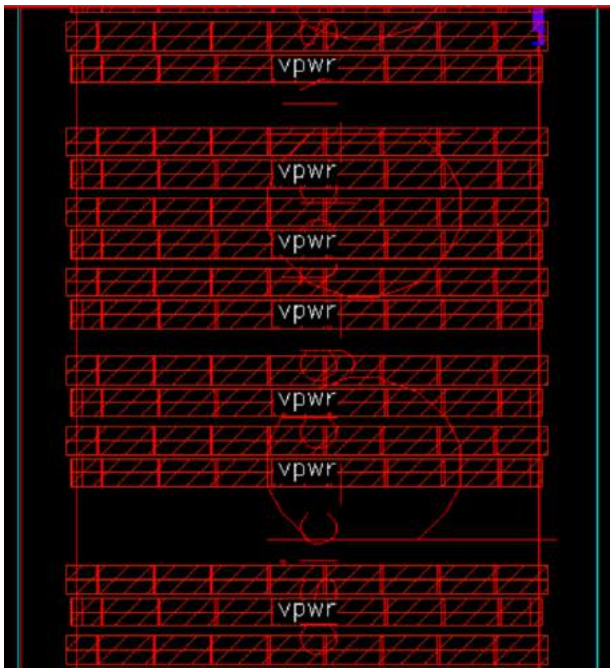
Current RF

CurrentRF PowerGrid

Up to 40% Digital and Dynamic Power Reduction
Creates Lowest Impedance Point in IC Power Grids
Dynamic Control of Reservoir Capacitance
PowerGrid Series Inductance Reduction
On-Chip EMI Reduction



General Description

The CurrentRF PowerGrid is an embedded Dynamic Power Reduction IP Suitable for Digital PowerGrid Overlays. The IP is intended to replace IC Power and Ground Digital PowerGrids leading to an almost zero IC area increase with PowerGrid integration. The IP features Capacitance Multiplication, Series Inductance Nullification, EMI Reduction, and Dynamic Power Energy Harvesting. The CurrentRF PowerGrid IP creates the lowest Impedance point in IC power grids aiding in maximum on chip supply line filtering, showing an up to a 600X improvement in effective and reservoir capacitance. The IP features a circuit noise activated dynamic input current controlled reservoir capacitance, and can function as a “stand-alone” on Chip DCAP, or work in parallel with existing DCAP structures. Due to the negative feedback embedded in the IP, the CurrentRF PowerGrid features a 25% reduction in effective series inductance (ESL). The IP operates by feeding back a portion (nominally 20%) of the bypass current flowing through chip input bypass capacitors, feeding back current onto the chip power grid, lessening bypass capacitor deep discharge, and thus less deep recharge from system supplies, thus reducing overall chip dynamic power draw. These effects substantially reduce RF Emissions from chip power grids making systems less vulnerable to cyber hacking and more secure. The IP draws no current for operation, thus maximizing block efficiency.

Topology

Ultra-Low Impedance Input Design
Single High Impedance Output
Bi-Directional Bypass Operation
Proprietary/Patented Topology

Features

40% Digital/Dynamic Power Reduction
On-Chip EMI Reduction
600X Increase in Effective Capacitance
25% Reduction in Capacitor ESL

Functional Description

The CurrentRF PowerGrid IP is a digital block Power Grid overlay with embedded feedback which is activated by dynamic noise current applied to it's Dvdd supply terminal. The embedded feedback creates conditions in which capacitive filtering is enhanced, normally thrown away current is recycled, and ESL is reduced, thus creating the lowest impedance point for noise in IC Power Grids.

Figure 1 shows the typical footprint of the CurrentRF PowerGrid IP. Figure 1 shows a typical Digital Block application. The IP block reuses the top level metal of the digital routing, forming a magnetic connection from the digital supply line. The IP structure follows a given digital block, and can be configured into almost any aspect ratio, giving it maximum versatility and flexibility in customer designs.
The IP is designed to be placed into the Digital PowerGrid on chips, achieving almost zero circuit area increase, and digital power reduction.

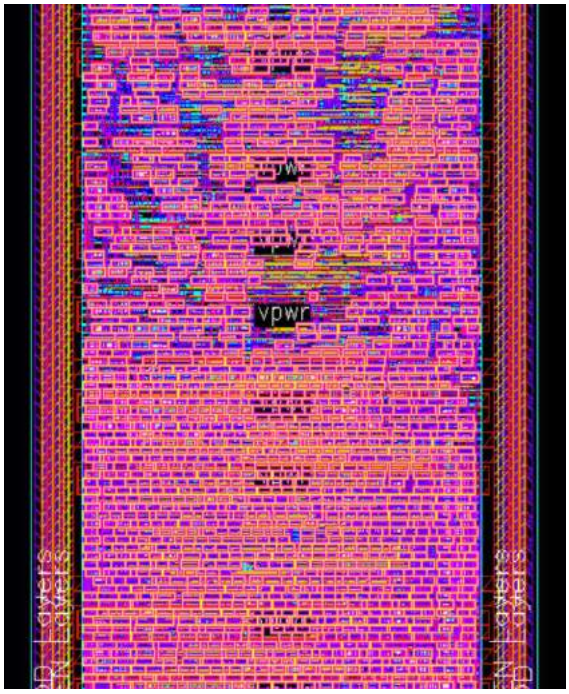
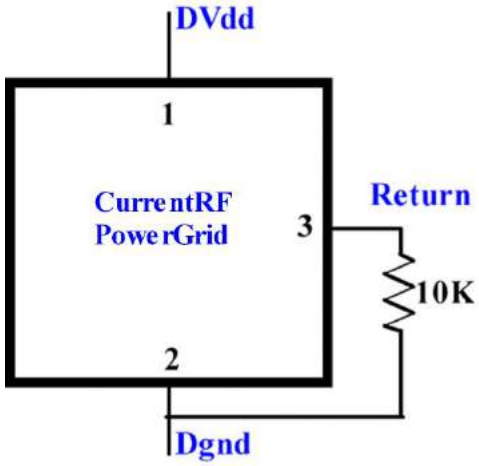


Figure 1: Example PowerGrid Footprint



Symbol	Pin	Type	Description
Dvdd	1	Power	Supply
Dgnd	2	Power	Ground
Return	3	Signal	Output Bias
			(Connect to 10K
			on-Chip Resistor)

Figure 2: CurrentRF PowerGrid Block Diagram and Pinout

Figure 2 shows the CurrentRF PowerGrid IP cell and pinout. Three connections are all that is needed for IP block operation. Dvdd and Dgnd are identical in function to conventional Digital PowerGrid and DCAPs. The return pin is connected to a 10K ohm on-chip bias resistor, the opposite end of the resistor connected to Dgnd.

Dynamic Power Savings Characteristics

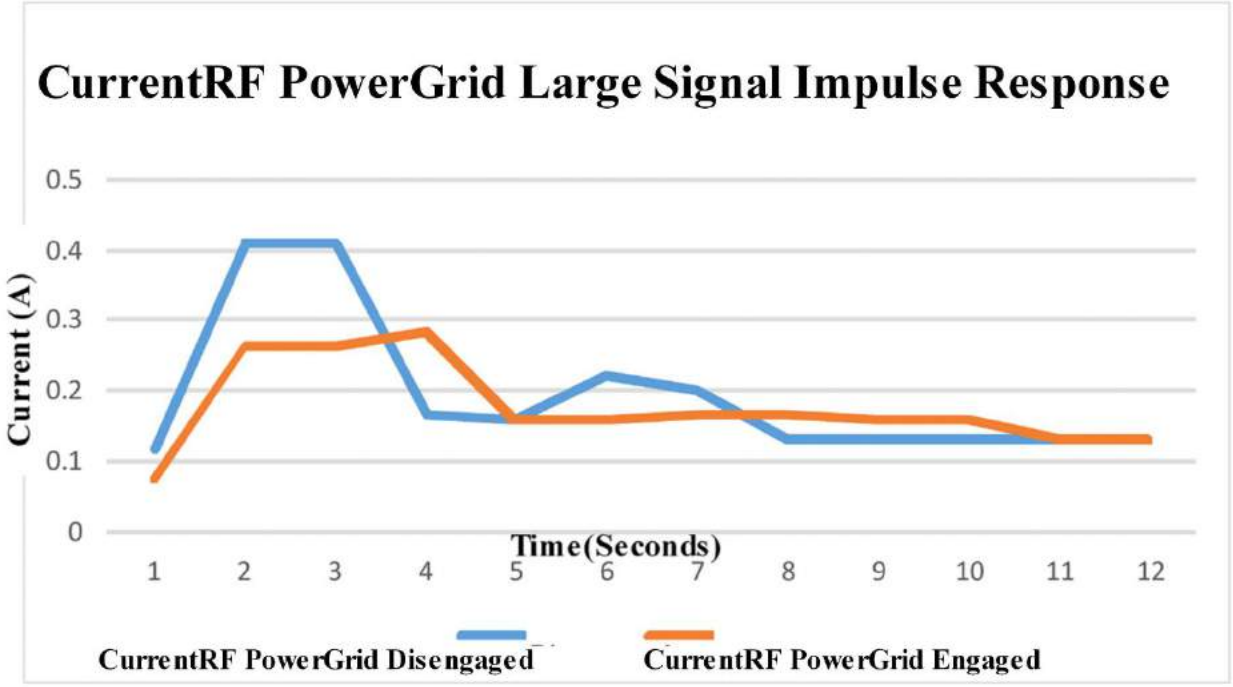


Figure 3: CurrentRF PowerGrid IP Cell Transient Surge Suppression Response

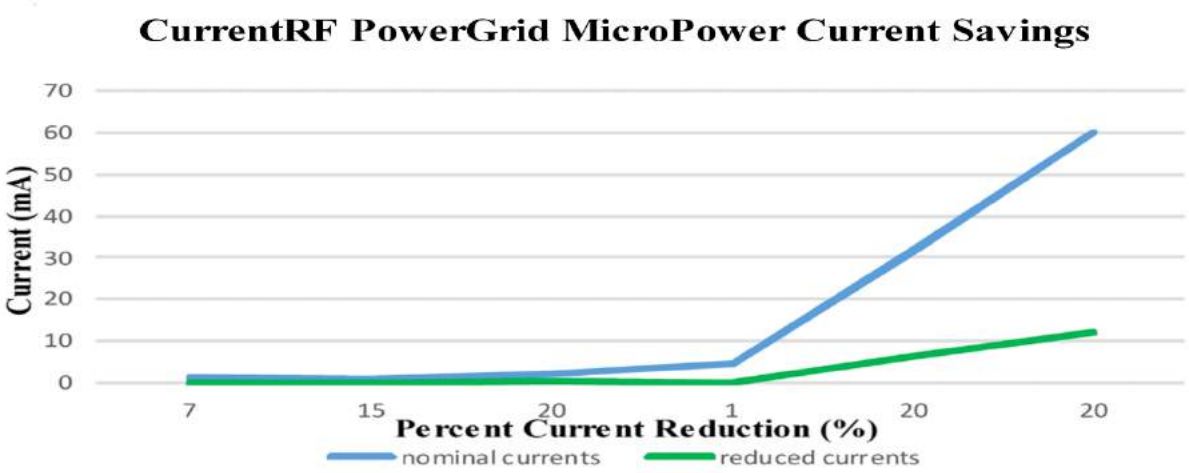


Figure 4: CurrentRF PowerGrid IP Cell Nominal Dynamic Current Reduction

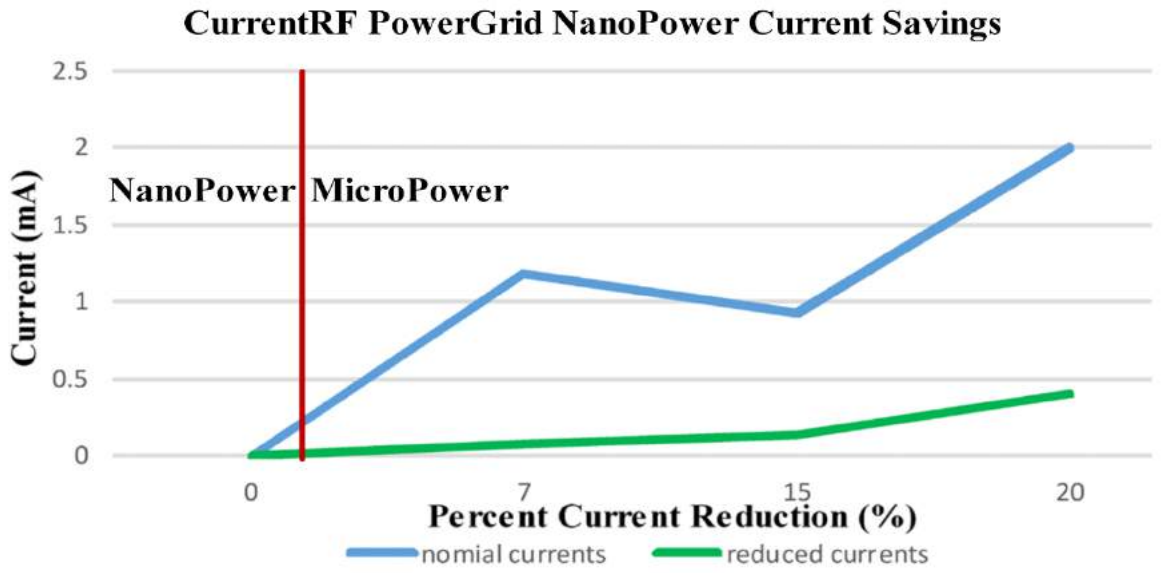


Figure 5: CurrentRF PowerGrid IP Cell MicroPower/NanoPower Dynamic Current Reduction

Figures 3, 4, and 5 detail the surge current, micro-power, and nano-power response and current savings of the CurrentRF PowerGrid IP. The percentage savings range from 40% to 10% savings dependent of conditions and nominal power level. Even at nano-power levels (250uA and below) 1% savings are realized when digital processing is turned on.

PowerGrid Lowest Impedance Point and Inductance Nullification

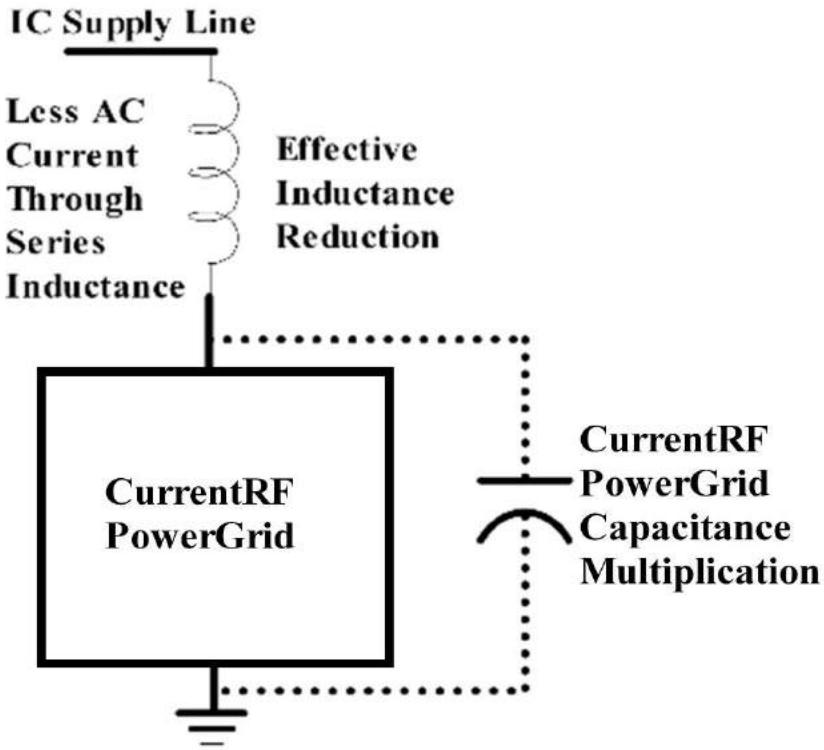


Figure 6: CurrentRF PowerGrid IP Effective Inductance Reduction and Lowest Impedance Point Generation

Figure 6 shows the electrical mechanisms that create the lowest impedance node in supply PowerGrids when utilizing the CurrentRF PowerGrid IP as PowerGrid Routing Overlays. The IP reduces the effect of power grid inductance by reducing the impulses created by switching overlap currents created by digital logic (Kirchoffs Current Law for AC, shown in Figure 6—less total AC current draw, less inductive reactance), and the effective capacitance increase (see Figure 8) plus the Capacitive Multiplication described in Figure 9. This lessening of inductive reactance and the increase in Dynamic Capacitance leads to a lower LC resonant frequency, pushing the lowest impedance point lower in the spectrum, which aids in attracting switching noise currents in the system, aiding the Dynamic Power reduction the CurrentRF PowerGrid IP affords.

Small Signal Broadband Impedance--Broadband Frequency Response

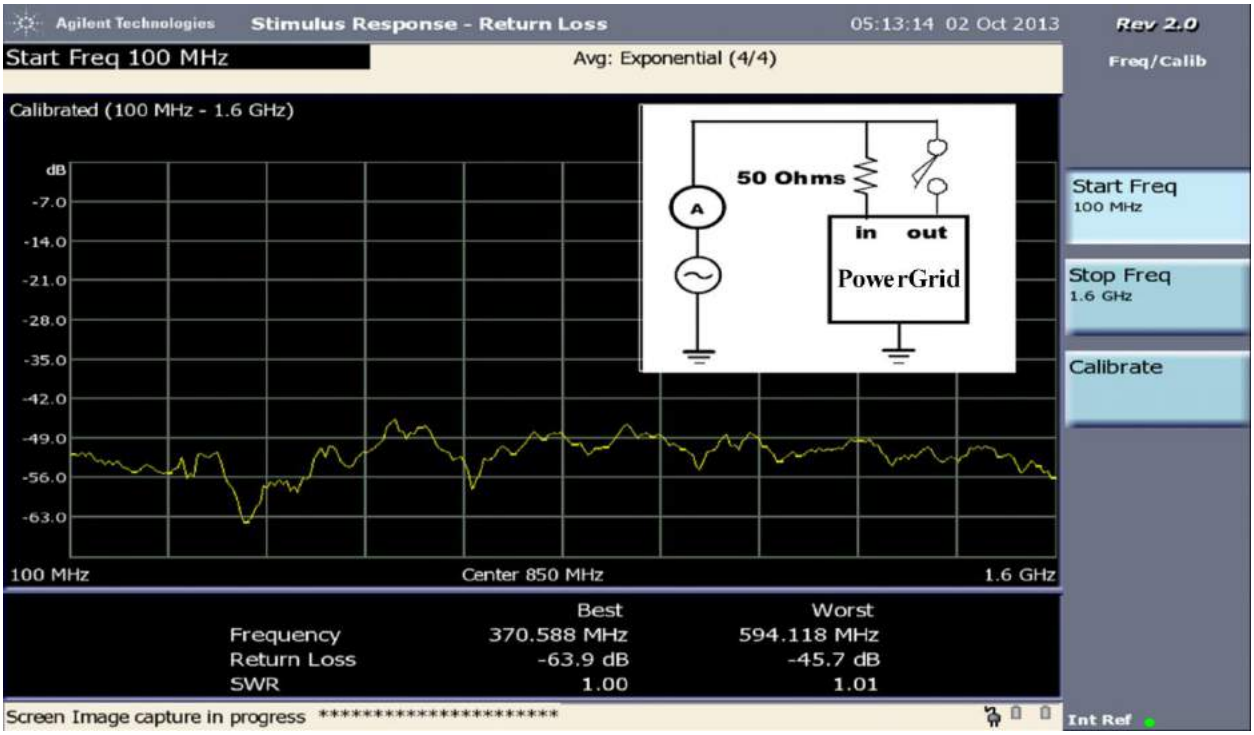


Figure 7: CurrentRF PowerGrid IP Small Signal S11 Input Plot (Disengaged)

The S_{11} return loss plot in Figure 7 graphically displays the bandwidth, input impedance, EMI suppression, and spectral response of the CurrentRF PowerGrid IP. The plot in Figure 7 shows a CurrentRF PowerGrid IP bandwidth ranging from 100Mhz to 1.6Ghz and the wideband S_{11} return loss of the device. With a series 50 Ω resistor placed at the input of the PowerGrid IP, as seen in Figure 7, the overall VSWR of the device input is quite good, varying from nearly perfect VSWR of 1.0 at 370Mhz, to a worst case VSWR of 1.01. The Figure 7 plot shows that the low input impedance of the device is negligible to the total input resistance, and does not show much variation over the input bandwidth of the IP.

In Figure 7, with the CurrentRF PowerGrid IP disengaged, looking exclusively into the on-chip input front capacitance (original on-chip DCAPs in this example), the best return loss/SWR and the lowest impedance point occurs at 370Mhz (-64dB) and corresponds to a capacitive low impedance magnitude of 39 Micro Ohms. A short math proof is as follows.

Equation 1:

$$50 * invlog\left(-\frac{dB}{10}\right) \cong 1/(2 * \pi * f * C)$$

Using the CurrentRF PowerGrid IP data, the lowest impedance point frequency in the Figure 7 plot, as well as the “Best” return loss and SWR numbers from the Network Analyzer, gives:

$$50 * invlog(-\frac{63.9dB}{10}) \cong 1/(2 * \pi * 370Mhz * of\ on\ chip\ DCAPs)$$

Solving yields:

$$20\mu\Omega \cong 39\mu\Omega$$

Which, within measurement and error tolerances, the results are essentially equal.

Narrowband spectral peaks and dips remain, however, in Figure 7, indicative of imperfections in the matching of the power grid on the IP evaluation board, test system cabling, and connectors.

The plot in Figure 8 shows the S_{11} spectral results of the CurrentRF PowerGid IP's negative feedback and power grid compensation. The Figure 8 plot demonstrates an increase in overall "returned" current (a 7 dB decrease in return loss, a slightly higher worst case VSWR of 1.03 vs. 1.01), but much reduced spectral peaks and dips, with respect to the plot in Figure 7. This return loss and VSWR decrease is not due to typical load mismatch effects, but is the result of CurrentRF PowerGrid IP action, returning current to the system for reuse. Thus, in the plot in Figure 8, the network analyzer power detectors show the device current return and negative feedback compensating for the imperfections present in the power grid on the CurrentRF PowerGrid IP evaluation board, test system cabling, connectors, etc.

Using the same input DCAPs as was used in the Figure 7 plot, and engaging the CurrentRF PowerGrid IP, the best return loss/SWR the transfer function lowest impedance point is translated down to 170Mhz(-56.3dB), as seen in Figure 8. Accounting for a +7 dBm scaling with respect to the Figure 7 plot, this due to return currents flowing from the CurrentRF PowerGrid IP output into the Network Analyzer detectors, the low impedance point corresponds to a capacitive low impedance of 42 Micro Ohms. This low impedance dip in Figure 8 fits the impedance and frequency characteristic that would be seen utilizing 2X the value of the on-chip input DCAPs. This measurement confirms the effective capacitance increase generated by the action of the CurrentRF PowerGrid DCAPs. The math for this condition as follows:

Equation 2:

$$50 * invlog((-dB - 7dB)/10) \cong 1/(2 * \pi * f * C)$$

Using the CurrentRF PowerGrid IP data, the lowest impedance point frequency in the Figure 8 plot, as well as the "Best" return loss and SWR numbers from the Network Analyzer gives:

$$\left(50 * invlog\left(\frac{(-56.3dB-7dB)}{10}\right)\right) \cong 1/(2 * \pi * 170Mhz * 2x\ of\ on\ chip\ DCAPs)$$

Solving yields:

$$23.4\mu\Omega \cong 42\mu\Omega$$

Which, within measurement and error tolerances, the results are essentially equal.

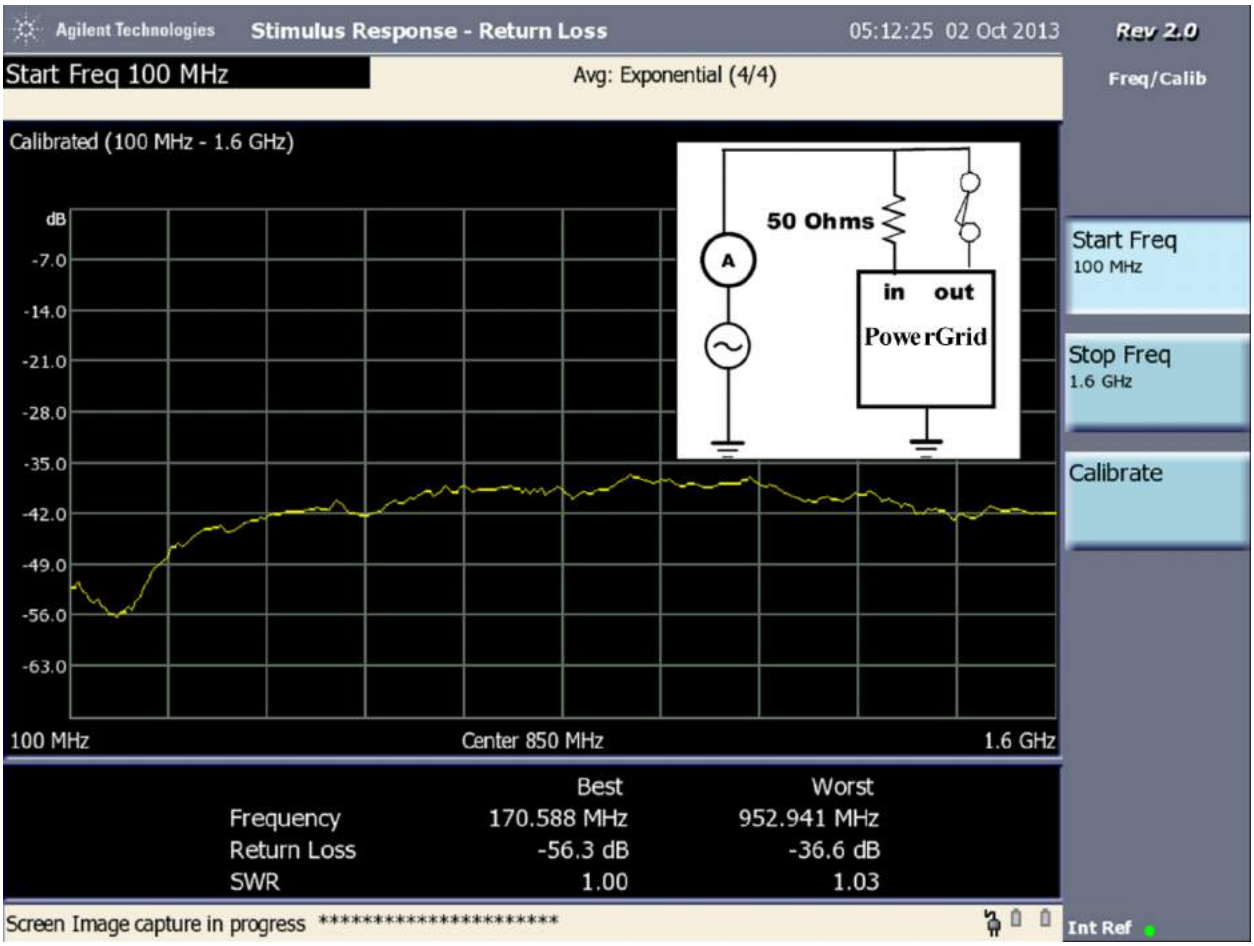


Figure 8: CurrentRF PowerGrid IP Small Signal S11 Plot (Engaged)

Large Signal Reservoir Capacitance Behavior

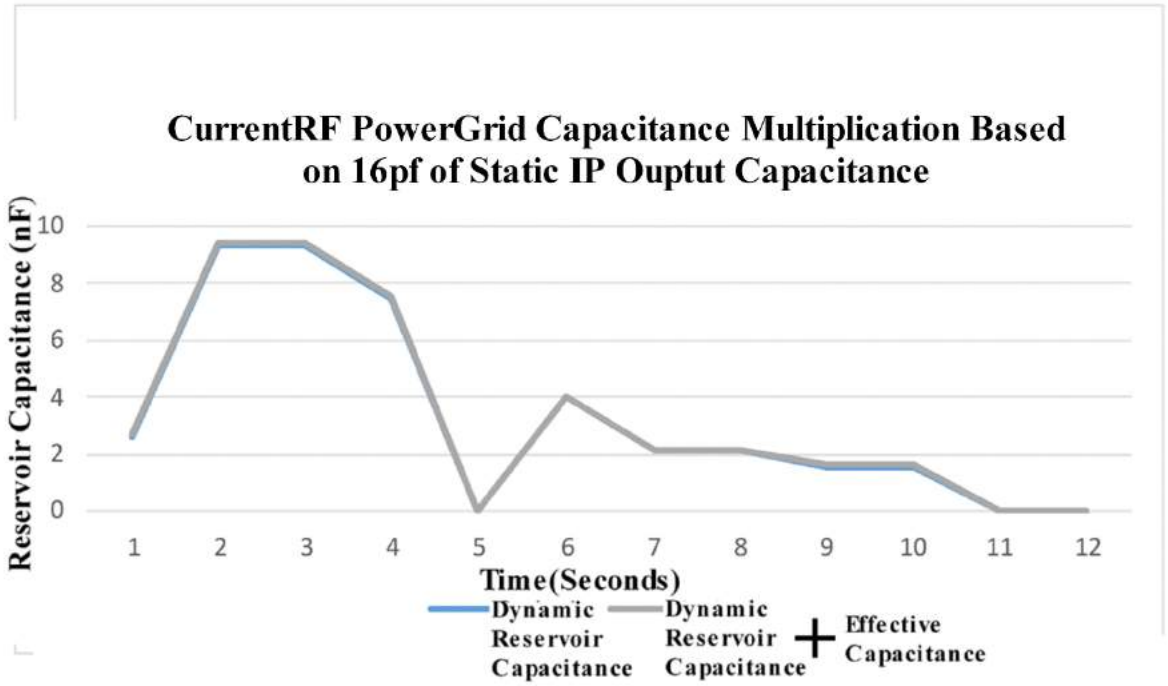


Figure 9: CurrentRF PowerGrid IP Dynamic Reservoir plus Effective Capacitance on chip IP Performance (16pf Static Output Capacitance)

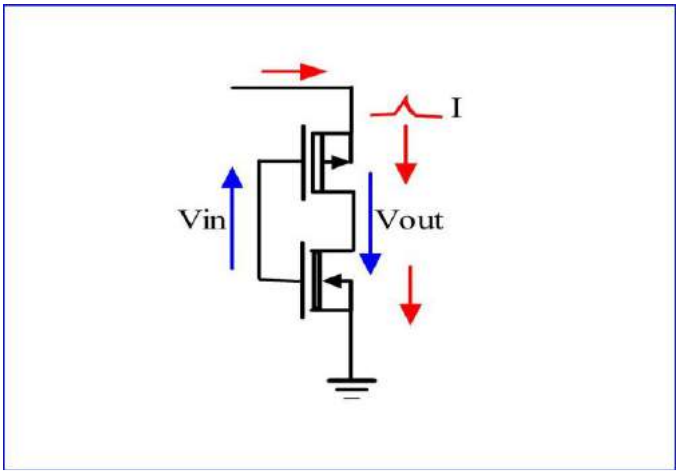
Figure 9 shows the total CurrentRF PowerGrid IP dynamic reservoir and effective capacitance increases that are the result of the load current impulses imposed on the system supply grid and the CurrentRF PowerGrid IP. The **grey** curve is the combination of the dynamic reservoir and effective capacitance, or total capacitance that the CurrentRF PowerGrid IP generates in response to high current impulses, the **blue** curve is the dynamic reservoir capacitance alone. As one can see, the dynamic reservoir capacitance magnitude far outweighs the effective capacitance, and the dynamic reservoir capacitance driven by the magnitude of input dynamic current and supply voltage perturbations.

With a 16pF static output or return capacitance used on the CurrentRF PowerGrid IP, the magnitudes of the reservoir capacitance approaches 10nF. This is almost an order of magnitude (600X) increase with respect to the capacitance provided by standard on chip MOS DCAPs. This is a good example of how the CurrentRF PowerGrid IP can dynamically enhance supply bypassing at the IC level of integration.

So**,** the 2X increase in small signal effective capacitance, the dynamically controlled increases in large signal, reservoir capacitance (600X), the 25% reduction in ESL, and the resulting 20% to 36% drop in overall Dynamic Current and Power Draw, leads to better high frequency (lower ESL) and low frequency (higher Effective and Reservoir Capacitance-- leading to better filtering capability) filtering (broader dynamic range), and an up to 20% reduction in dynamic power draw. These characteristics lead to lower RF emissions from power grids, cleaner internal chip supplies, smaller DCAP footprints(if filtering area is a concern) lower chip dynamic power dissipation(lower thermal footprint), and greater circuit capacity.

RF EMISSIONS & WASTED ENERGY in Integrated Circuits-The Root Cause

Much energy is wasted in IC chip design, a portion of this waste radiating into free space. In the attempt to keep digital supply lines clean from the noise effects created by high frequency surges of overlap current in CMOS based logic, IC decoupling/reservoir capacitors are used to shunt this current to ground, thus keeping on-chip supplies clean. This current is generally ignored by chip designers, and is treated as “throw away” or ignored current and energy. Unless on-chip supplies are corrupted beyond a 50mV limit, this current is discarded and ignored.



Overlap current will not be ignored, however. Not only is it the source on dynamic power dissipation in chip designs, it shows up spectrally, radiating into space from power grids in ICs, giving away important system information, allowing hackers to gain access and compromise data.

CMOS logic based overlap current flow is the primary source of dynamic power dissipation in digital and mixed signal ICs. If even a small portion of this current can be recovered and reused, chip power dissipation is reduced and data is made more secure.

Figures 10 through 14 are various examples of CC-100IP RF Emission and dynamic power reduction on various processes and circuit architectures.

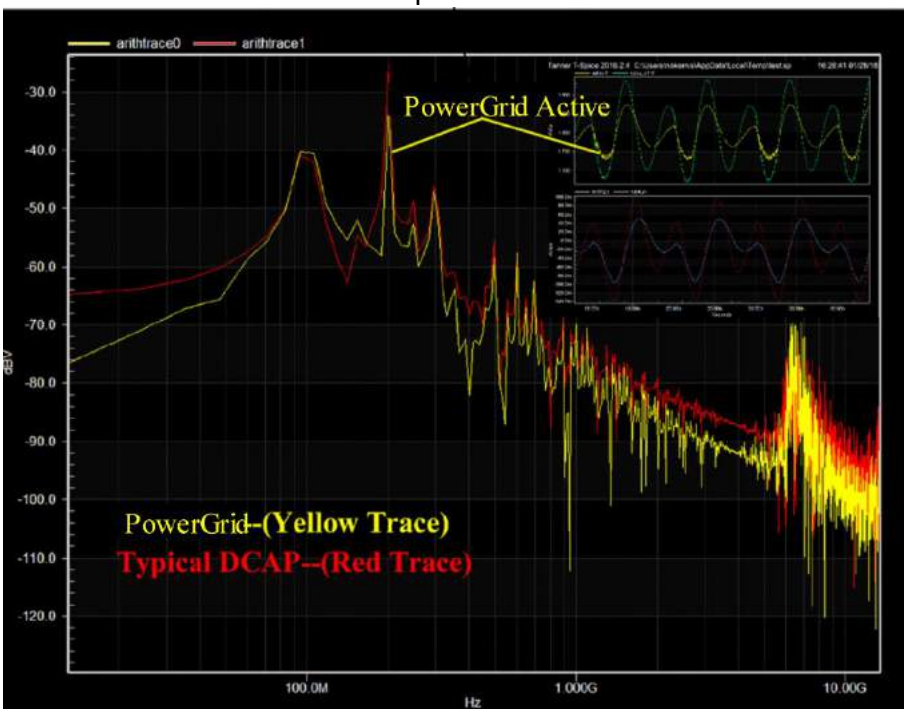


Figure 10: CurrentRF PowerPad IP Noise Magnitude Reduction (Manufacturing Process: Jazz Semiconductor CA18)

The plot in Figure 10 features not only a drop in overall emissions (the **yellow** curve in Figure 10), but also a 6dB drop in radiated emissions at 200Mhz, which translates to a 75% attenuation of power grid radiated energies(a quarter power point).

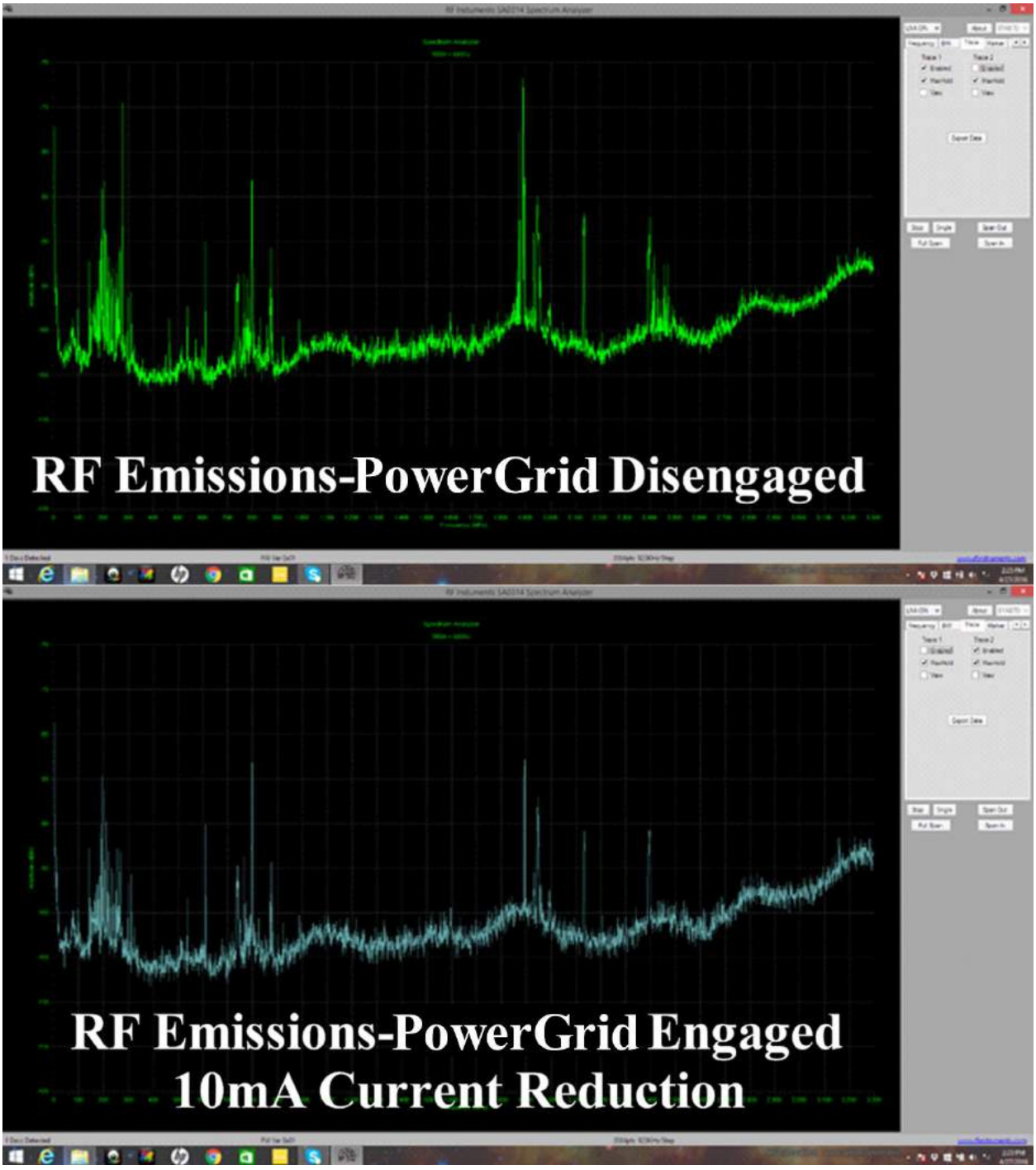


Figure 11: CurrentRF PowerGrid IP Embedded in a Server Ethernet Controller (prototype)

The Figure 11 plot also shows an overall drop in radiated emissions due to CurrentRF PowerGrid IP feedback, featuring a 12 dB drop (a 16X reduction) in radiated emissions at ~1.9Ghz. The overall current saved from this reduction in dynamic current is ~10mA.

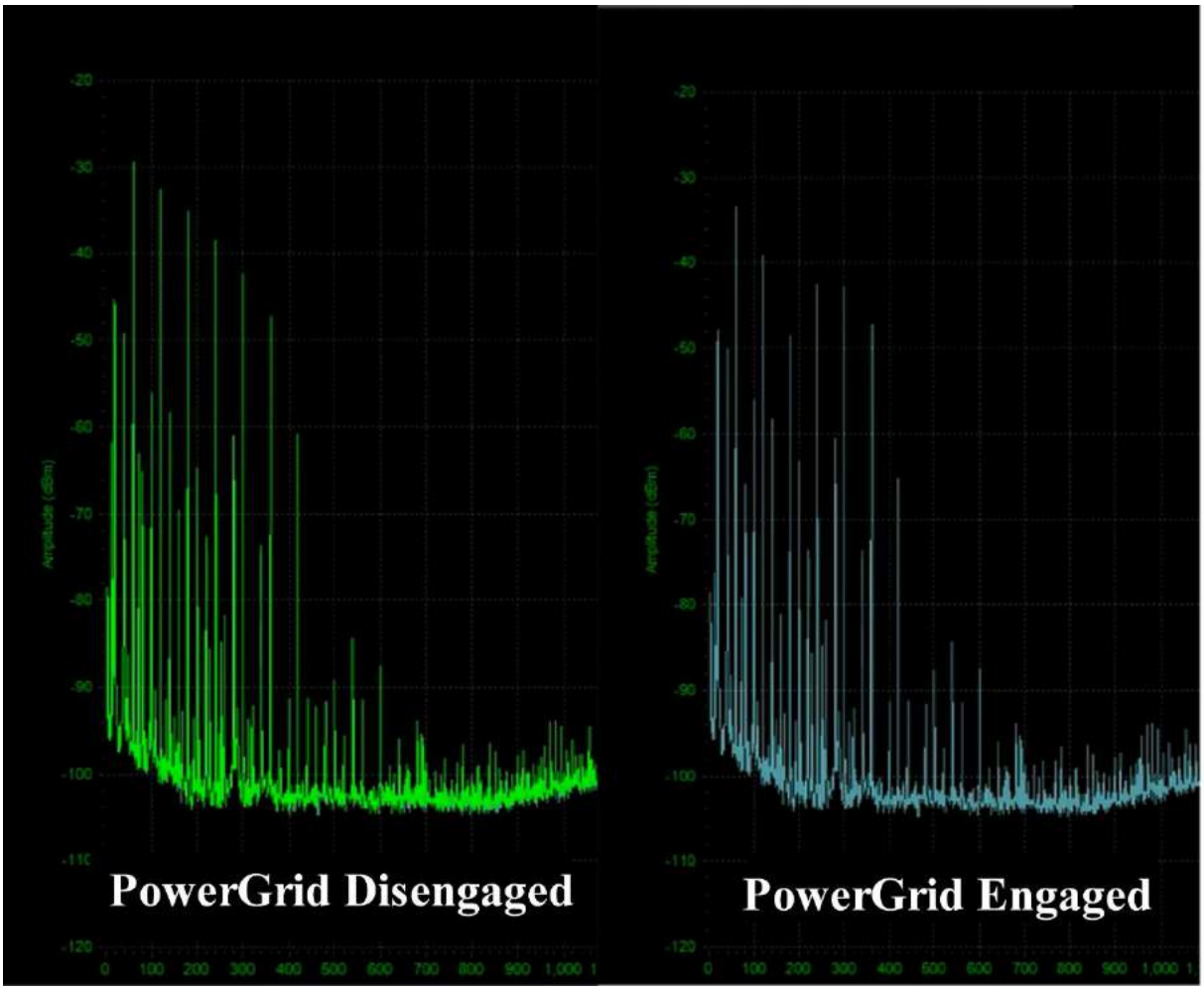


Figure 12: CurrentRF PowerGrid IP Test Chip Results-20% Current Reduction (Manufacturing Process: GF_018RF)

Figure 12 shows a 6 dB (half power point) broadband RF Emission reduction in a square wave spectrum measured on the CurrentRF PowerGrid IP test chip. A 20% dynamic current reduction was seen as the result of the emission reduction.

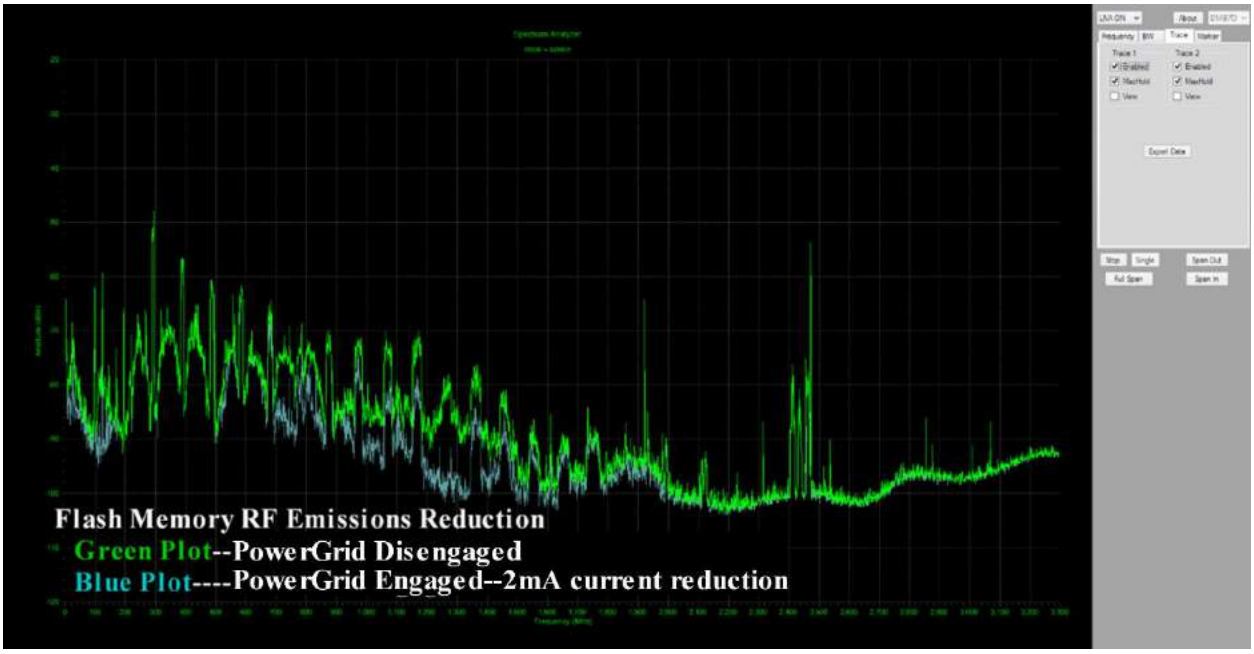
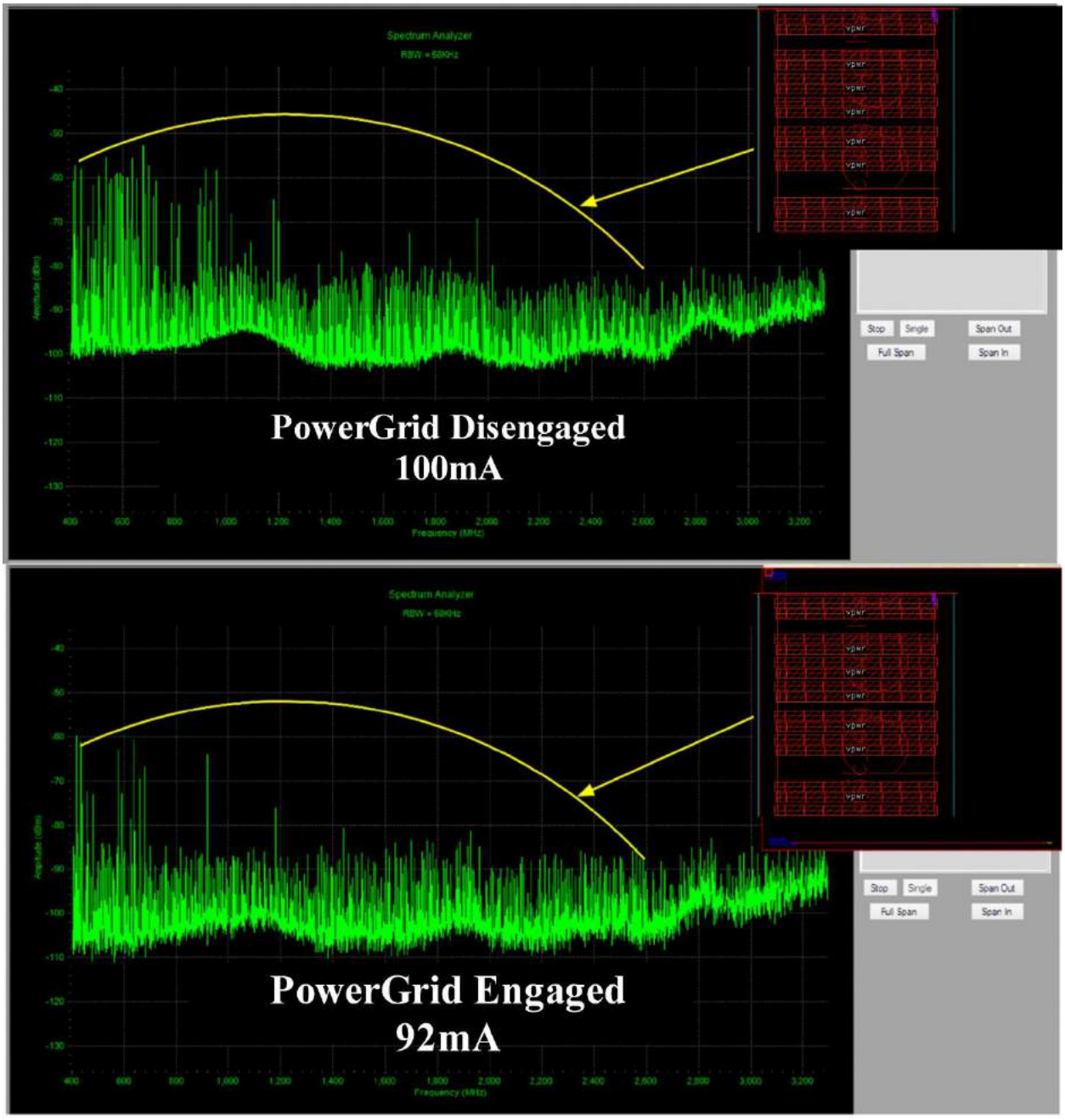


Figure 13: CurrentRF PowerGrid IP embedded in Flash Memory

Figure 13 shows the disengaged/engaged RF emission spectrums that are the result of the CurrentRF PowerGrid IP embedded in a flash memory power grid. A 2mA dynamic current reduction is seen as the result of PowerGrid IP activity.



Missing/Suppressed Frequencies Above
Equals Cancelled Emissions and Current Saved

Figure 14: CurrentRF PowerGrid IP embedded in a Pseudo Random Generator Test IC (Manufacturing Process: GF_018RF)

Figure 14 demonstrates an 8 mA dynamic current reduction that is the result of CurrentRF PowerGrid IP RF Emission reduction as a consequence of PowerGrid IP activity on the power grid of a pseudo random test generator produced by CurrentRF. The pseudo random test generator chip was designed to not only test the CurrentRF PowerGrid IP, but demonstrate the ability of the IP to be integrated into larger digital circuits.

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